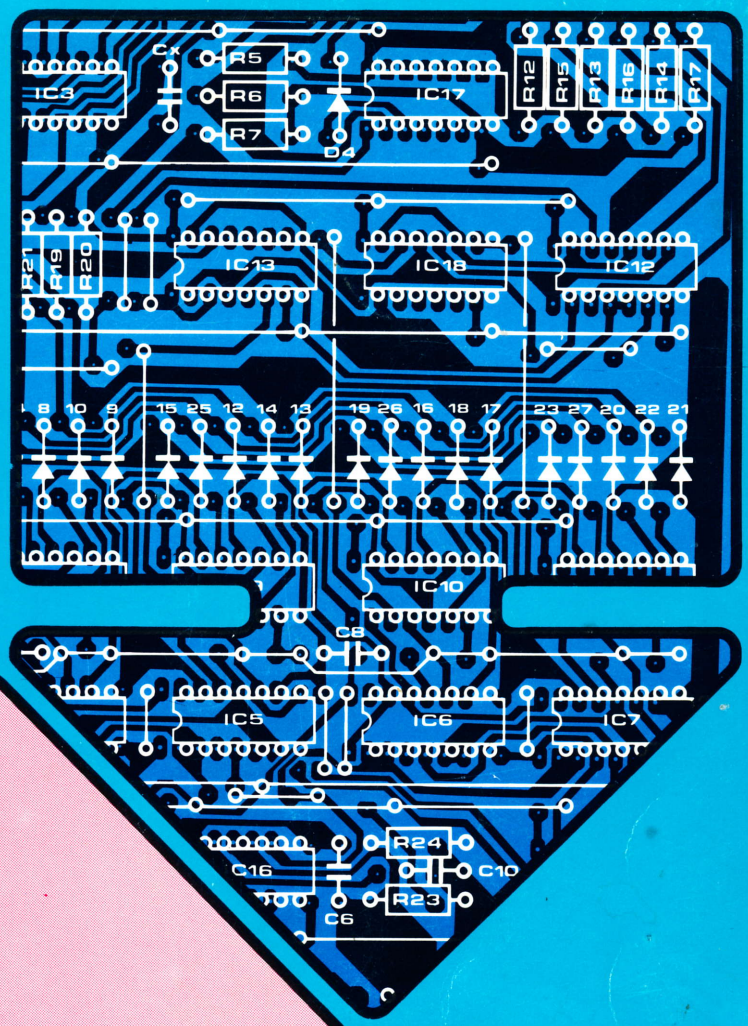
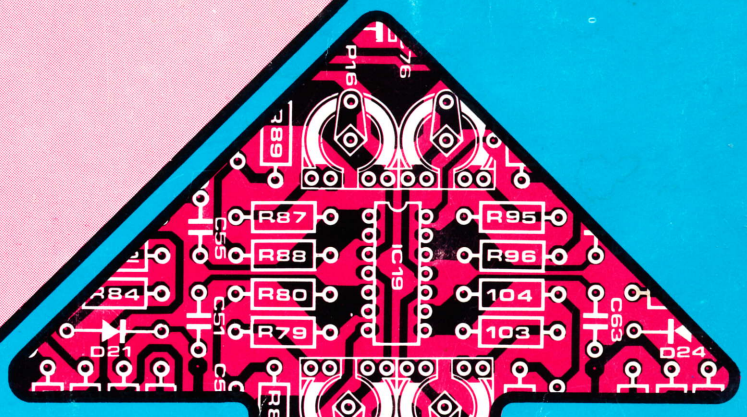
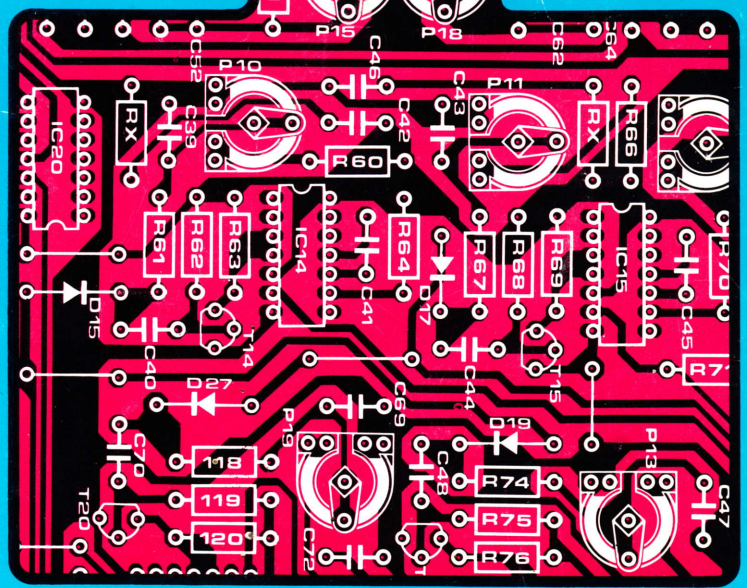
ELEKTOR BOOK 75







A selection of some of the most interesting construction projects in volume 1 (1975) of ELEKTOR magazine.

A selection of some interesting construction projects, originally published in ELEKTOR issues 1 to 8.

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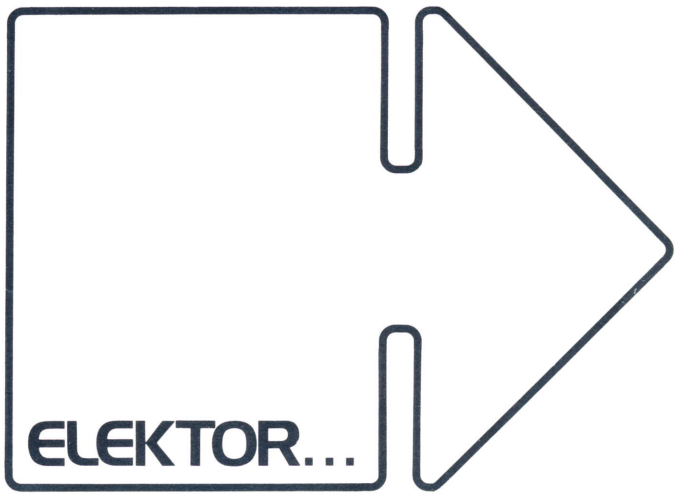

. . . . . is an electronics magazine with a difference. New components, new ideas and new developments in the field of electronics are used in practical designs.
This stimulates the professional designer to up-date his knowledge of electronics; on the other hand, even the beginning amateur should be able to build most of the projects.
Ready-made printed circuit boards are available for many of the designs.

THIS BOOK...

. . . . . contains a selection of interesting projects which were originally published in Volume 1 (1975).
We have taken the opportunity to clarify some points that have given rise to technical queries in the past. For those who are not yet accustomed to the Elektor style of writing, we would like to draw particular attention to pages 18, 19 and 106.

ELEKTOR BOOK 75

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1	3 4	5 6

1. circuit title
3. board number
4. * = p.c.b.'s with solder mask
5. price (in £) inclusive of VAT
6. + = 12.5% VAT; otherwise 8% VAT

versatile digital clock	4414B	1.50
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clamant clock, striking system	4015-27	1.45
disc preamp 76131	4040A	1.15+
recip-riaa	4039	0.90
stylus balance	9343	0.45+
aerial amplifier	1668	1.25+
miniature amplifier	1486	0.60+
mos clock 5314 clock circuit	1607A	1.80
mos clock display board	1607B	1.30
mos clock timebase	1620	0.90
univeral frequency reference	HD4	1.50
edwin amplifier	97-536	1.35+
compressor	6019A	1.60+
car anti-theft alarm	1592	1.85

CONTENTS

versatile digital clock

'One-chip' digital clocks, such as the MM5314 are excellent for simple time-keeping, however, they are not ideal for driving external devices such as time signals, calendars, etc. This is where this 'conventional' clock design can really be useful. This clock uses standard TTL IC's, has a BCD-coded time output, as well as pulse train outputs giving repetition rates varying from one second to one per day. Several external devices that can be used with this clock are described further on ('Clamant clock' and 'calendar').

Elsewhere in this book there is a design for a 'one-chip' digital clock, with both mains and crystal reference frequencies. Whilst ICs such as the MM5314 are excellent for simple timekeeping, they have certain disadvantages. Since the output to the display is multiplexed the time output of the clock is not easily accessible in a parallel form. This means that the clock is unsuitable for driving time-controlled devices such as alarms, calendars, central heating programming, automatic recording of radio programmes or other systems. The clock described in this article is based on TTL circuitry and is eminently suitable for control systems. The time is available as a BCD coded output, and clock pulse trains with rates varying from one a second to one a day are obtainable. Many constructors will probably have some of the ICs in their 'junk box'.

The complete circuit of the clock (excluding power supply) is given in figure 1. The basic operation is quite simple. With all the switches in the positions shown the clock runs normally. The 50 Hz input is rectified by D1, clamped to 4.7 V by D2 and then fed into the NAND Schmitt trigger ST1. A 50 Hz square wave suitable for driving TTL appears at the output of ST1 and is fed to IC10 which is connected as a divide-by-five counter. Asymmetric 10 Hz pulses are available at the 'D' output of IC10. These pulses are fed to IC9, which is connected as a divide-by-10 counter. A symmetrical 1 Hz square wave is available at output 'A' of this IC.

The 1 Hz pulses are fed to IC6, which is connected as a BCD decade counter. This counts seconds from 0 to 10 and the BCD output may be decoded for display using a 7447. The 'D' output of IC6 produces one pulse every ten seconds, and this is fed to IC5, which is connected as a divide-by-6 counter. This counts tens of seconds from 0 to 6. When the tens of seconds count reaches 6 (i.e. the seconds display changes from 59 to 60) the BCD output of IC5 is 0110, that is to say the 'B' and 'C' outputs of the IC are both '1'. These outputs are connected to the Reset 0 inputs, so that when the count reaches 6 IC5 is reset instantaneously, and the 6 display is never seen.

One pulse per minute is obtained from the 'C' output of IC5, and this is fed through N2 and N1 to IC4, which is again connected as a BCD decade counter.

The time-setting circuits around N1 and N2 will be discussed later.

Like IC5, IC3 is connected as a divide-by-6 counter, so that it counts tens of minutes.

Counting of the hours is slightly more complicated. Since the clock is a 24 hour design, the hours counter (IC2) must count up to 10 twice, then reset at 4 on the third count sequence (i.e. when the hours count reaches 24). Since the tens of hours counter only counts to 2 a counter is made up from two JK flip-flops (7473) instead of using a 7490. Resetting is accomplished as follows: During the first 0-10 count of IC2 the Q outputs of FF1 and FF2 are low. When the 'D' output of IC2 goes low on the tenth count the Q output of FF1 goes high. At the end of the second count sequence the Q output of FF1 goes low and the Q output of FF2 goes high. The Q output of FF2 and the 'C' output of IC2 are connected to the Reset 0 inputs of IC2, so that when IC2 reaches 4 in its third count sequence it is reset. However FF2 cannot similarly be reset as it has no gating on the clear input. This difficulty is overcome by feeding the 'B' output of IC2 to the clear input of FF2 via C1 and R3. On count 4 of IC2 the 'B' output goes low, feeding a momentary reset pulse to FF2. Of course this occurs at count 8 also, and during the first and second count sequences. However, it is only during the third count sequence that the Q output of FF1 is high anyway, so these earlier reset pulses do not matter, since the flipflop is reset already.

The capacitive coupling (C1, R3) is necessary to ensure that only a short reset pulse is provided. If direct coupling were used then the clear input would be held low on count 10 during the second count sequence, and the Q output of FF2 could not go high.

Provision of 'tick'

It will be noted that IC9 is connected differently from the other divide-by-10 counters (IC2, IC4 and IC6). This is because a BCD output is required from the other counters. IC9 is connected to give a symmetrical square-wave output, as a convenient simulated 'tick', and this happens to sound better with a 1:1 mark-space ratio.

Time-setting

Three time-setting switches are provided. Two to make the clock advance at a fast rate, and one to stop the clock. This is useful because the clock can be set to a particular time, stopped, then the stop button can be released exactly on the time signal from radio or telephone. It is also handy if the clock is accidentally advanced too far as it saves going all the way 'round the dial'. Gating for the time-setting is provided by a 7400 (IC7) plus the spare half of the 7413 Schmitt trigger (½IC8).

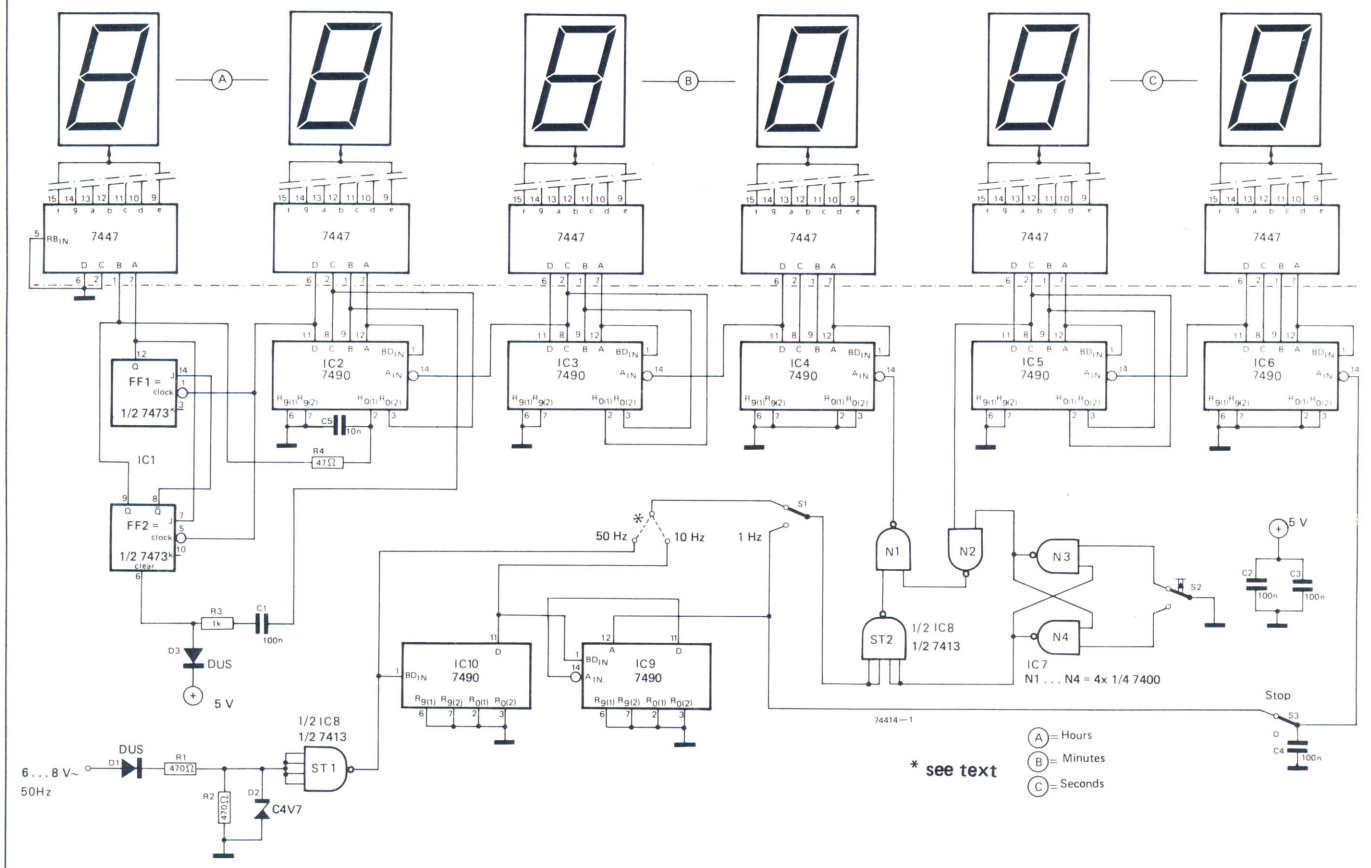
The operation is as follows: when S2 is in the position shown in figure 2a the set-reset flipflop N3/N4 is reset, so the output of N3 is high and the output of N4 is low. This means that the output of ST2 is high. Pulses from output 'C' of

Figure 1. Circuit diagram of the clock. The printed circuit board does not include the display and its associated decoder/drivers.

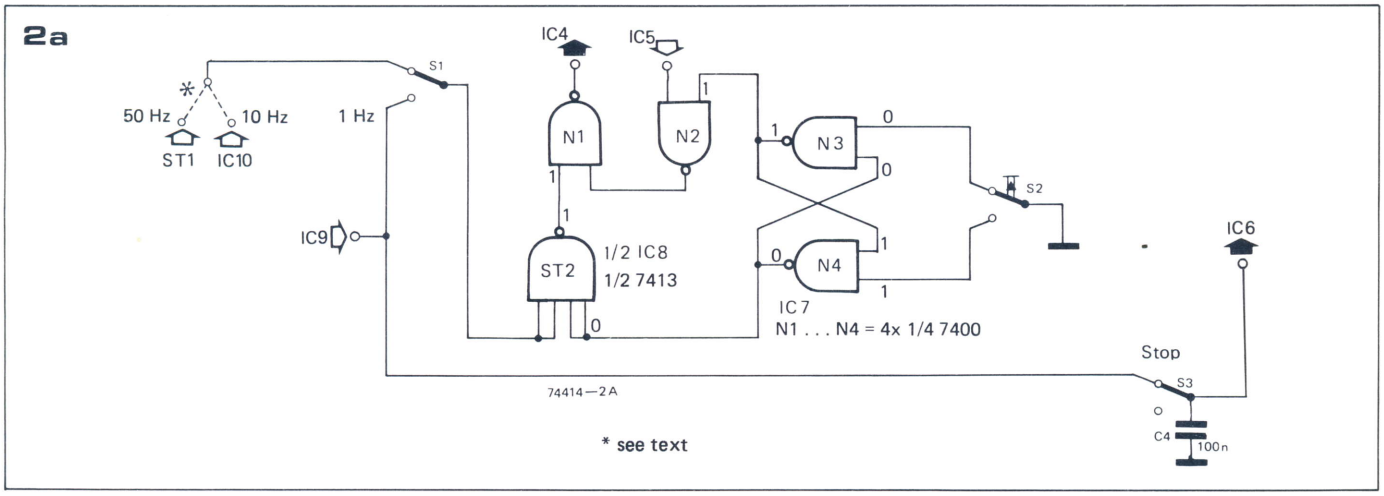
Figure 2a. Logic levels at NAND gates for normal timekeeping.

Figure 2b. Logic levels at NAND gates for time-setting.

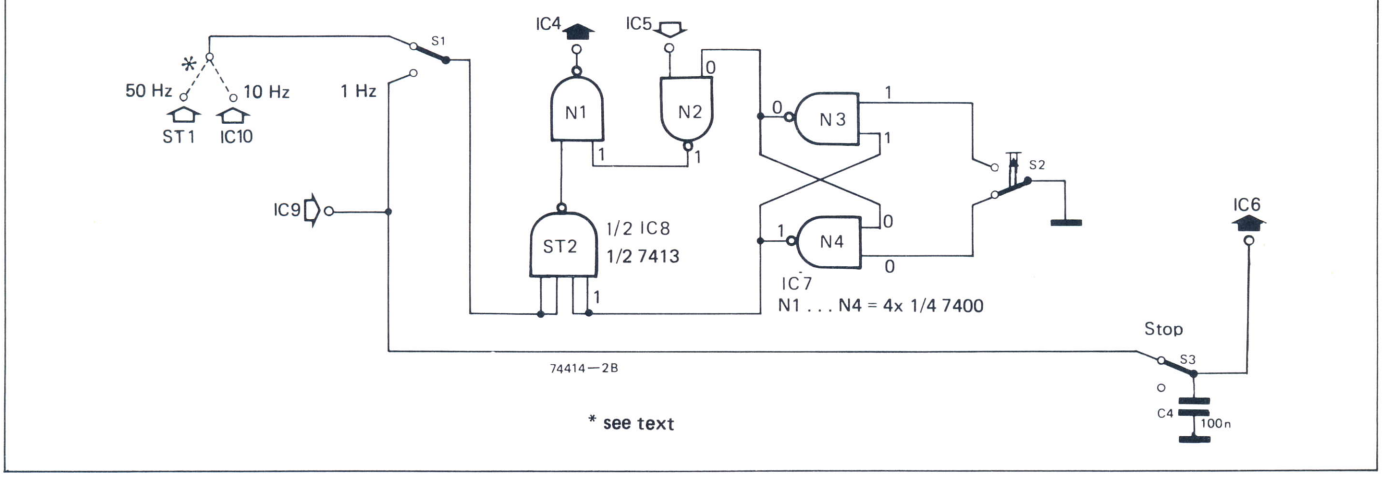
1


7447
IC1
FF1 = 1/2 7473
FF2 = 1/2 7473
IC2 7490
IC3 7490
IC4 7490
IC5 7490
IC6 7490
IC7
N1 . . . N4 = 4x 1/4 7400
1/2 IC8 1/2 7413
ST1
ST2
IC9 7490
IC10 7490
50 Hz
10 Hz
1 Hz
S1
S2
S3
Stop
5 V
DUS
C4V7
6 . . . 8 V~
50Hz
74414—1
* see text
A = Hours
B = Minutes
C = Seconds

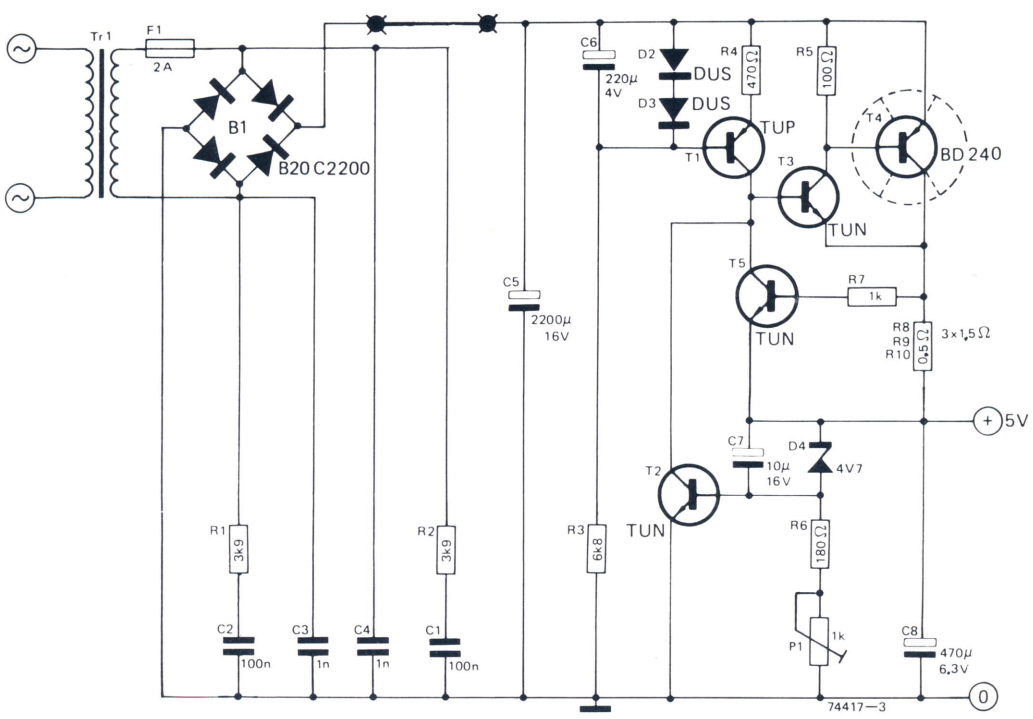
2a


IC4
IC5
IC6
IC9
S1
S2
S3
50 Hz
10 Hz
1 Hz
ST1
IC10
N1
N2
N3
N4
ST2
1/2 IC8
1/2 7413
IC7
N1 . . . N4 = 4x 1/4 7400
Stop
C4
100n
74414—2A
* see text

2b


IC4
IC5
IC6
IC9
S1
S2
S3
50 Hz
10 Hz
1 Hz
ST1
IC10
N1
N2
N3
N4
ST2
1/2 IC8
1/2 7413
IC7
N1 . . . N4 = 4x 1/4 7400
Stop
C4
100n
74414—2B
* see text

3



Parts list

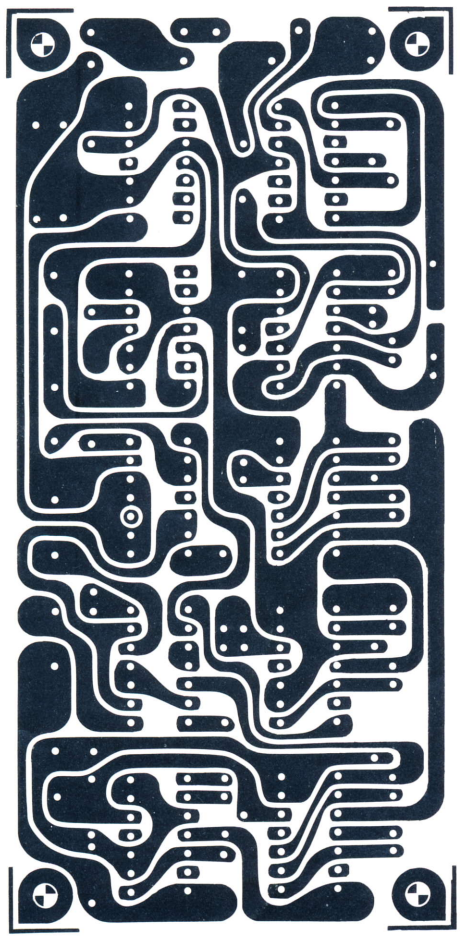
Resistors:
R1,R2 = 470 Ω
R3 = 1 k
R4 = 47 Ω

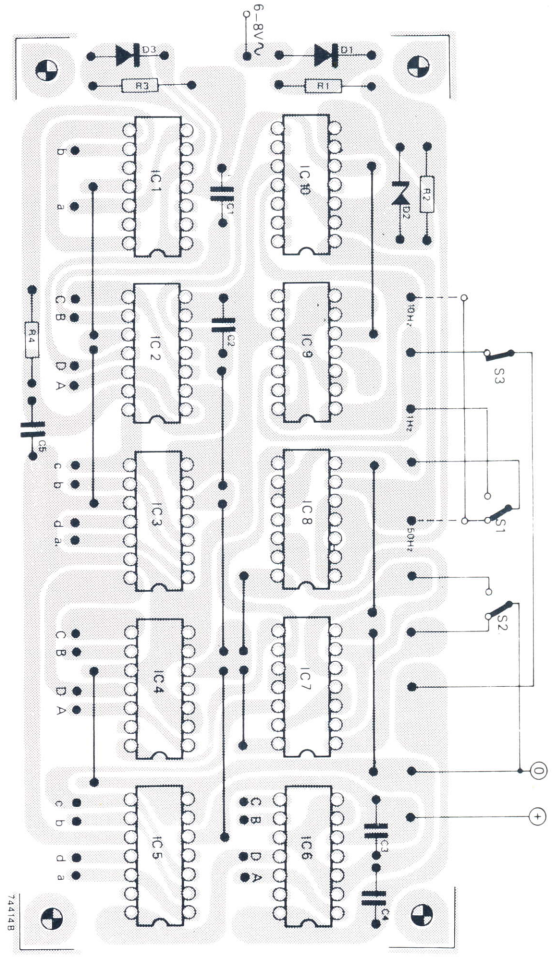
Capacitors:
C1,C2,C3,C4 = 100 n
C5 = 10 n

Semiconductors:
IC1 = 7473
IC2 ... IC6,IC9,IC10 = 7490
IC7 = 7400
IC8 = 7413
D1,D3 = DUS
D2 = Zener 4V7

Switches:
S1 = Single-pole, 2-way
S2 = Single-pole, 2-way, push-button operated
S3 = Single-pole on-off

4





IC5 are thus transferred through N2 and N1. When S2 is changed over (figure 2b) the flipflop is set. The output of N3 is low and the output of N4 is high. The output of N2 therefore goes high. 1 Hz or 10 Hz pulses (depending on position of S1) are now transferred through ST2 and N1 to the input of IC4. The clock will therefore count at the rate of one minute per second or 10 minutes per second. As an alternative to the 10 Hz rate, 50 Hz pulses may be used. This rate is useful only for setting the hours rapidly.

The flipflop is necessary to suppress contact bounce on S2. The flipflop is set (or reset) when the switch initially makes contact on being changed over. Subsequent switch bounce will not affect the state of the flipflop.

When S3 is changed over the 1 Hz drive is disconnected from IC6 so the clock stops. The position of S3 during time-setting with S2 is unimportant.

Power Supply

The clock requires a supply of about 1 A at 5 V. As transient interference on the mains supply could interfere with the timekeeping of the clock a stable, well-filtered mains supply is essential. The circuit of figure 3 is recommended, as this can deliver up to 2 A and is well stabilised. The 50 Hz drive for the clock can be derived from either side of the transformer secondary winding.

Construction

The p.c. board and layout for the clock are given in figure 4, and the assembly requires little comment. The BCD outputs of the counters are brought out to the edge of the board. Display decoding is not provided on the board. Suitable decoder and display boards are the 'Universal Display' (see following pages). If zero suppression on the tens of hours display is required pin 5 of the 7447 should be grounded.

The layout and p.c. board of the power supply are given in figure 5. The output voltage of the supply should be set to 5 V before connecting to the clock.

For 60 Hz operation, see the following page.

For use with crystal time base, see 'Universal time base'.

Parts list

Resistors:
R1,R2 = 3k9
R3 = 6k8
R4 = 470 Ω
R5 = 100 Ω
R6 = 180 Ω
R7 = 1 k
R8,R9,R10 = 1.5 Ω
P1 = 1 k, preset

Capacitors:
C1,C2 = 100 n
C3,C4 = 1 n
C5 = 2200 μ/16 V
C6 = 220 μ/4 V
C7 = 10 μ/16 V
C8 = 470 μ/6.3 V

Semiconductors:
B1 = Bridge rectifier, e.g. B20C2200
D1 = omitted
D2,D3 = DUS
D4 = zener 4.7 V, 400 mW
T1 = TUP
T2,T3,T5 = TUN
T4 = BD240 or equ.

Sundries:
F1 = 2 A delay-action fuse
Tr1 = transformer, 8 V/2 A

Table 2

Clock Pulse Number	FF1		FF2			LED display
	Input J1 (14) connected to $\overline{Q2}$	Output Q1 (12) BCD Code A	Input J2 (7) connected to Q1	Outputs Q2 (9) BCD Code B	Outputs $\overline{Q2}$ (8)	
1	1	0	0	0	1	0
	1	1	1	0	1	1
2	0	0	0	1	0	2
3	1	0	0	0	1	0

Table 1. BCD code.

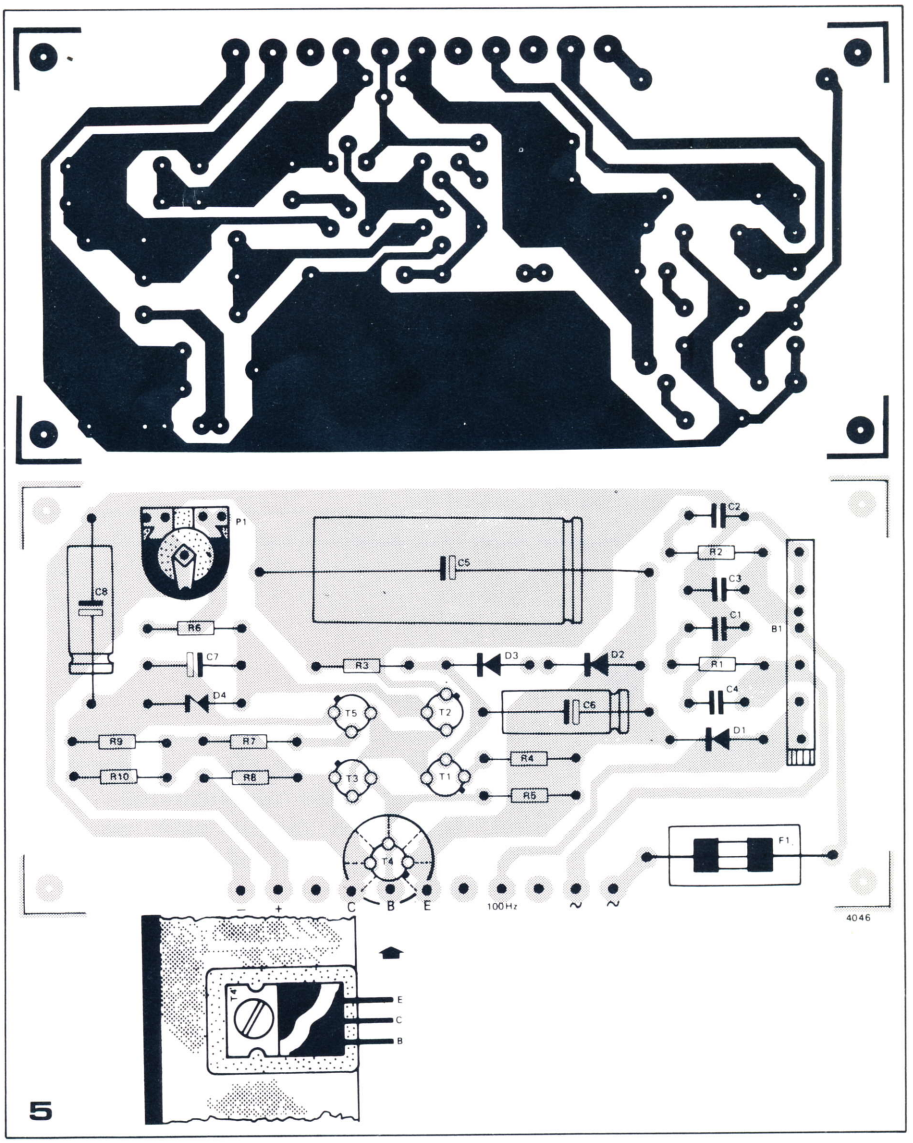
COUNT	INPUTS D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Table 2. Truth table for IC1 (7473 connected as 1:3 divider).

Figure 3. Circuit of 5-V stabilised power supply.

Figure 4. Printed circuit and component lay-out of the clock.

Figure 5. Printed circuit and component lay-out of the 5-V stabilised power supply.



universal display

It is frequently necessary to have available a numeric display for many projects such as frequency counters, digital voltmeters etc. It is a tedious and untidy business to build up such displays on matrix board, so Elektor have designed a universal display which should satisfy the requirements of most enthusiasts. The display may be used with seven-segment LED indicators.

The universal display is modular in construction and its basic form consists of a board to accomodate two displays and their associated decoders. The system may be extended to any number of digits and decade counter/latch boards may also be added.
The universal display uses the popular 7447 decoder. The display format of this decoder is given in figure 1. However, for digits 6 and 9 the improved format described in Elektor 2, p. 258, is employed. This is shown in figure 2. The basic configuration of the decoder with the additional transistors is shown in figure 3 and the complete circuit of a display module for use with LED displays is given in figure 4.

Construction

Double-sided boards are employed in the construction of the display module and it may be seen from figures 5 and 6 that components are mounted on both sides of the board. It should be emphasised here that great care is required in the assembly of these boards due to the degree of miniaturisation involved. The soldering iron must have an extremely fine tip and soldering must be done extremely quickly to avoid peeling the fine track from the board. The boards available from Elektor employ plated- through holes, so that it is unnecessary to solder to component leads on both sides of the board. Simply solder on the opposite side of the board to that on which the component is mounted.

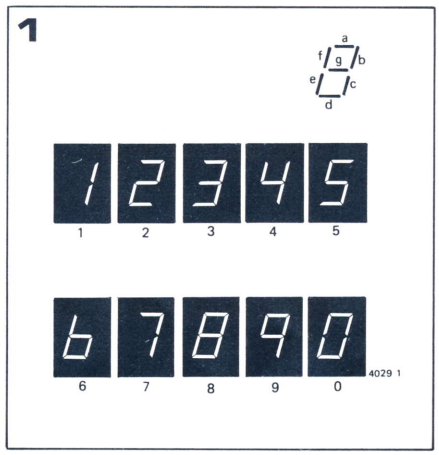


Figure 1. The display format produced by the 7447 decoder.

Figure 2. The improved presentation of the digits 6 and 9 as used in the universal display.

Figure 3. The circuit used with the 7447 to achieve the improved 6 and 9 display.

Figure 4. Circuit of the LED version of the universal display. Note that the decimal point series resistor has a higher value than the segment resistors to achieve the same luminous intensity.

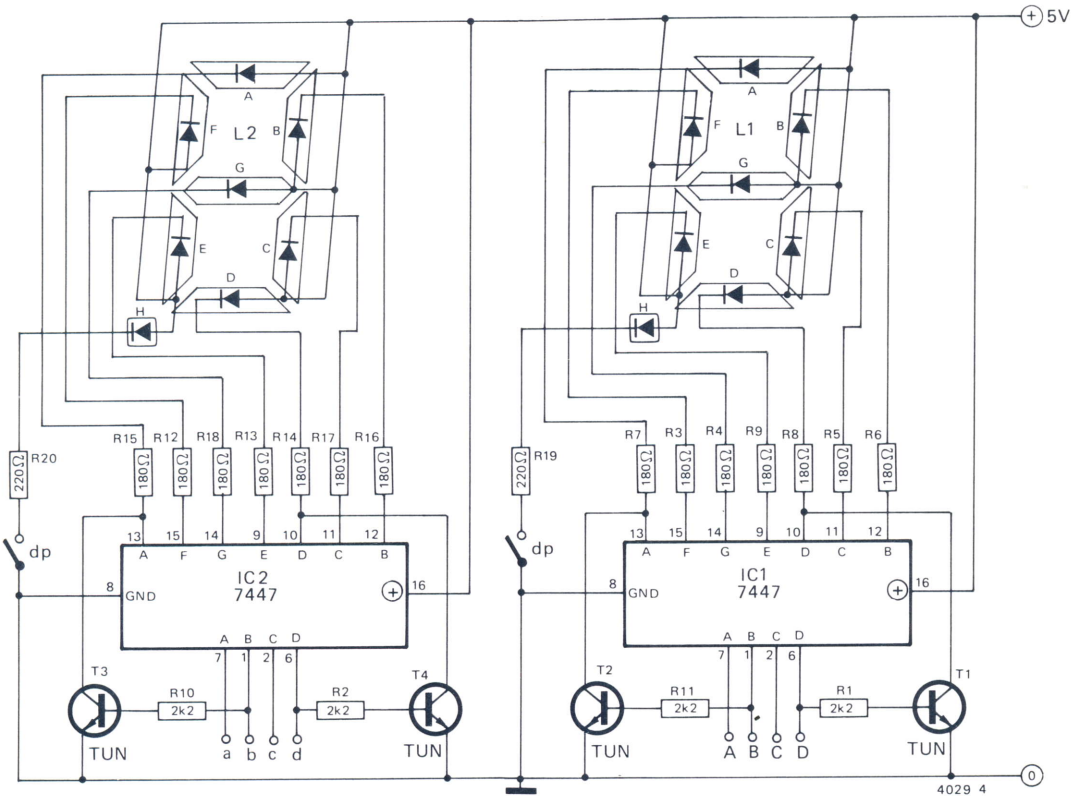
Figures 5 and 6. The p.c. board and layout for the LED display. The track shown in feint in the component layouts is the side of the board on which the components are mounted, i.e. the components are mounted directly on top of the track shown. Figure 5 shows the components on the back of the board, and figure 6 shows the display side. (EPS4029-2).

versatile digital clock

60 Hz operation

The versatile digital clock can be used in countries that use 60 Hz mains by making a few simple modifications.
First: break the circuit path on the p.c.b. between pin 11 of IC10 and pin 1 of IC9.
Then: connect a jumper wire between pin 8 of IC10 and pin 1 of IC9.
Finally, use a 7492 for IC10.

4



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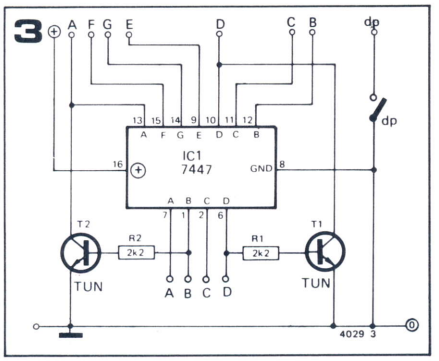
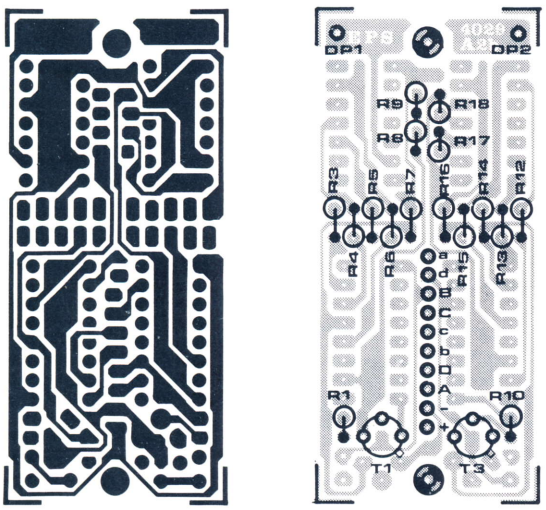


Components list for figure 4:

Resistors:
R1,R2,R10,R11 = 2k2
R3 to R9, R12 to R18 = 180 Ω

Semiconductors:
T1 to T4 = TUN
IC1,IC2 = 7447
L1,L2 = e.g. H.P.5082-7730 or 7750, Opcoa SLA 1, T.I. Til 302, Data Lit DL 707.

5



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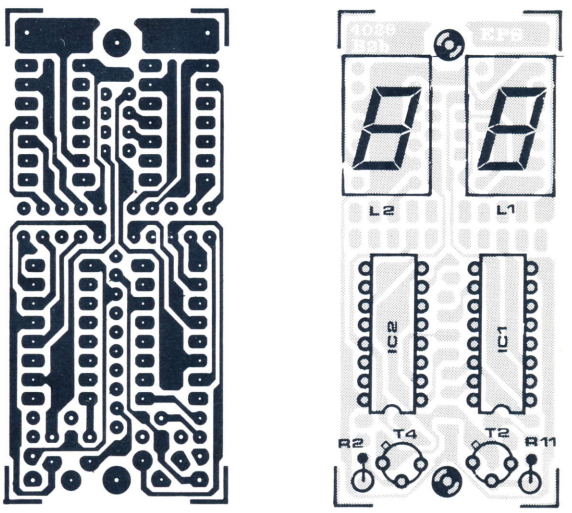
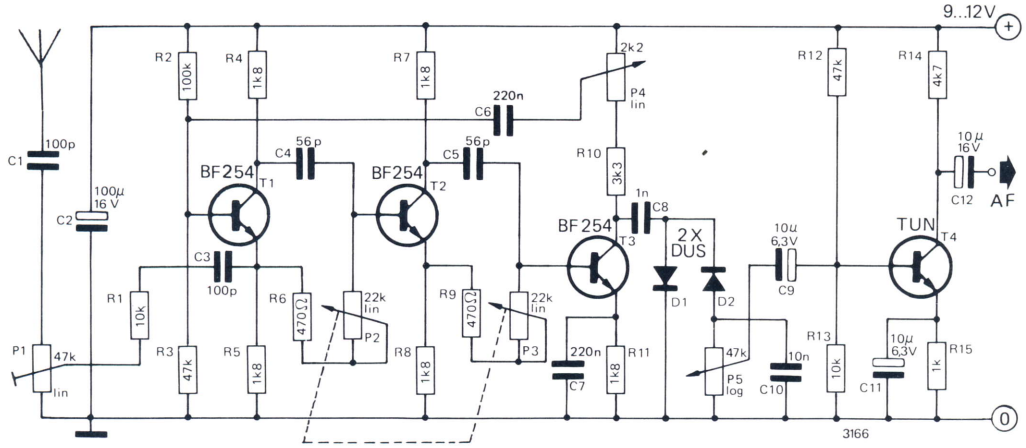


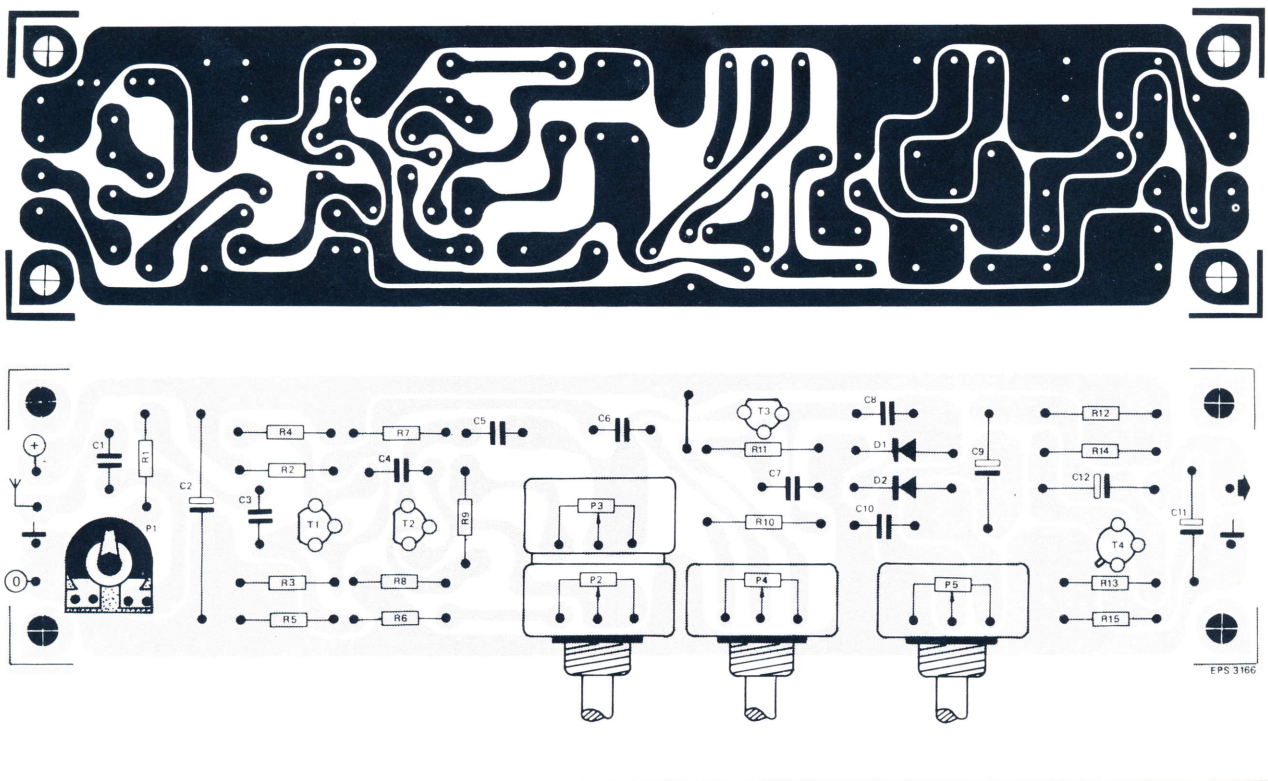
sensitive coil-less synchrodyne receiver for MW and LW

This little receiver tunes the medium and long wave-ranges. It operates without any coils by employing a synchronised oscillator.
When the oscillator is barely able to maintain oscillations, it will synchronise to an incoming signal frequency close to its free-running value. The amplitude of the oscillation follows, more or less linearly, the modulation of the incoming signal. The circuit can synchronise itself to a signal of some tens of microvolts, so that its effective sensitivity is very high.

P4 sets the level of oscillation; the stereo-ganged pair P2 and P3 form the 'tuning' control. Since this stereo-potentiometer covers a very wide range it may be necessary to add a 'fine' control consisting of a low-value stereo-potentiometer in series (typically 1 k or 500 ohm).
The modulated oscillator signal is passed to the amplifier stage with T4, via the full-wave 'detector' with D1 and D2. The output level is sufficiently high for driving most amplifiers.

A short aerial, such as a piece of wire, is enough to provide quite reasonable reception. If a good aerial is to be used, P1 can be inserted to prevent over-driving by too strong a signal.





mini hifi

In contrast to the now-prevalent 'multiwatt' systems currently on the market, a design is described for a Hi-Fi stereophonic amplifier of modest specification for the price-conscious constructor. The system is built from several units that are matched to one another, but this does not preclude their use with other equipment.

The block diagram of figure 1 shows how the units are connected together to form a complete stereo amplifier. The disc preamplifier is required only with a magnetic cartridge. It is followed by the control amplifier which incorporates balance, volume and tone controls. This stage will accept inputs from high level sources such as radio and tape.

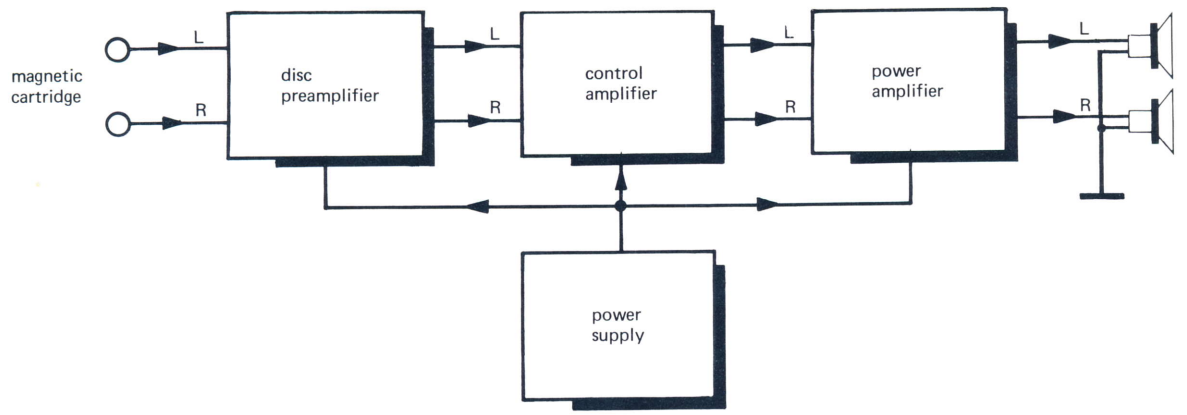
The control amplifier drives the power amplifier which will provide up to 3 watts per channel; this is sufficient for the average living room. A regulated power supply provides the H.T. for all three stages of the amplifier.

The disc preamplifier

The disc preamplifier, the circuit of which is given in figure 2 (one channel only shown), incorporates equalisation to correct the output of a magnetic cartridge according to the RIAA playback curve, and also amplifies the signal to a level sufficient to drive the control amplifier. It consists of a two-stage voltage amplifier, T4 and T5, with the RIAA feedback network R18, R19, C15 and C16 connected from the collector of T5 to the emitter of T4. DC feedback and biasing of T4 is provided by R15.

The disc preamplifier board should preferably be mounted inside the turntable itself as otherwise the capacitance of the screened lead between the cartridge and the disc preamplifier can form a resonant circuit with the self-inductance of the cartridge. If this resonance lies within the audio spectrum it may cause a peak in the frequency

1



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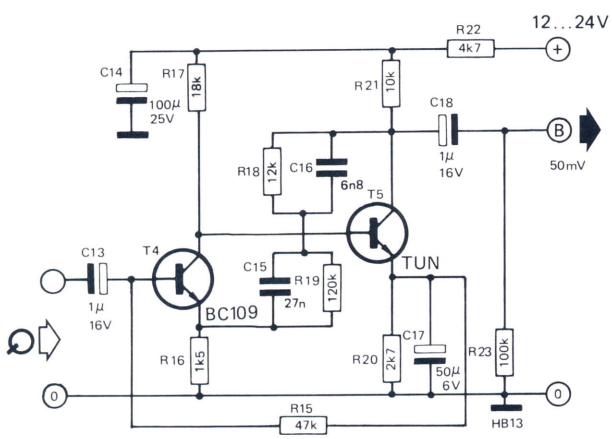
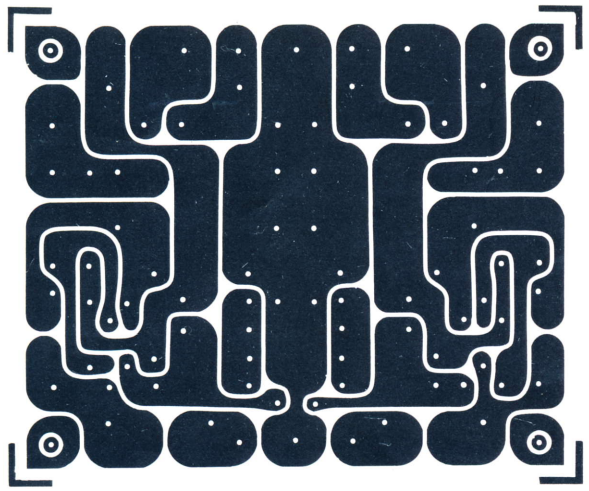


Figure 1. An economical Hi-Fi stereo amplifier built of four units. Each unit may also be used in conjunction with other equipment.

Figure 2. The circuit of the disc preamplifier. It is designed for use with magnetic cartridges and incorporates RIAA correction.

3



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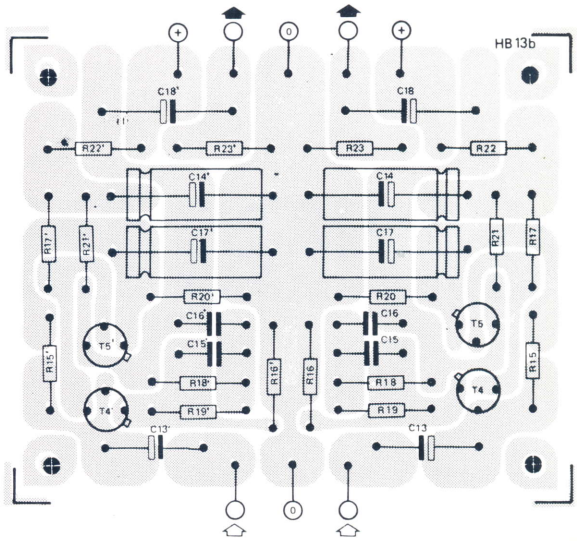

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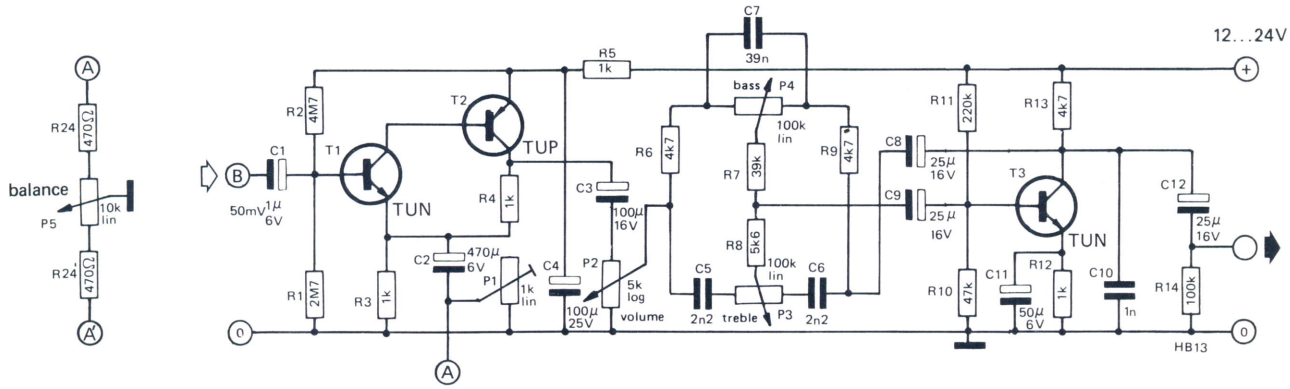


response. Of course some cartridge manufacturers quote a recommended load capacitance and if this is so their recommendations should be adhered to. Another good reason for mounting the disc preamplifier inside the turntable is to keep it away from the hum fields of the amplifier's mains transformer. Turntable motors usually have much less stray field then the average mains transformer!

The printed circuit board for the disc preamplifier is given in figure 3 and the associated component layout in figure 4. It can be seen that the layout for the two channels is symmetrical.

The control amplifier

The circuit of one channel of the control amplifier is given in figure 5. T1 and T2 form a voltage amplifier with a high input impedance and a low output impedance. Two versions of the power amplifier are described in the following section; a 12-volt version, to give 3 watts into 4 Ω and a 17-volt version, to give 3 watts into 8 Ω. Since the output voltage of the amplifier for 3 watts into 4 Ω is 3.5 V RMS, whereas for an 8 Ω load it is 4.9 V RMS, the 17-volt version of the power amplifier requires a larger input signal, since its gain is fixed. This is accomplished by varying the gain of the control amplifier by means of P1. P1 is also used to match the gains of the two channels so that channel balance is correct with the balance control central. With P1 set to 1 k the input sensitivity when used with the 12 volt version of amplifier is about 150 mV for 3 watts into 4 Ω.

P2 is the volume control and this is followed by a standard 'Baxandall' tone control circuit which gives a range of ±12 dB on both bass and treble. The balance potentiometer P5 completes the controls. C10 is a high-frequency bypass capacitor to avoid instability. The p.c. board and component layout of the control amplifier are given in figures 6 and 7.

The power amplifier

In the circuit of figure 8 T1 and T2 form a direct-coupled voltage amplifier which controls the bias of the quasi-complementary driver/output stage T3, T5 and T4, T6. R7 and R8 are chosen so that the output devices are either just biased on or just cut off depending on the gain of the devices used. C3, C5 and R3 help to maintain stability. The input sensitivity of the amplifier is about 400 mV for 12 volt operation with a 4 Ω load, and 600 mV for 17 volt operation with an 8 Ω load. The gain

Figure 3. The layout of the p.c. board for the disc preamplifier shows the symmetrical arrangement of the two channels. (EPS HB14).

Figure 4. The component layout for the disc preamplifier board of figure 3.

Figure 5. The circuit of one channel of the control amplifier.

Figure 6. The printed circuit for the control amplifier. (EPS HB13).

Figure 7. The component layout of the control amplifier.

Parts list for figures 2 and 4:

Resistors:
R15 = 47 k
R16 = 1k5
R17 = 18 k
R18 = 12 k
R19 = 120 k
R20 = 2k7
R21 = 10 k
R22 = 4k7
R23 = 100 k

Capacitors:
C13 = 1 μ, 6 V
C14 = 100 μ, 25 V
C15 = 27 n
C16 = 6n8
C17 = 50 μ, 6 V
C18 = 1 μ, 16 V

Semiconductors:
T4 = BC 109
T5 = TUN

Parts list for figures 5 and 7:

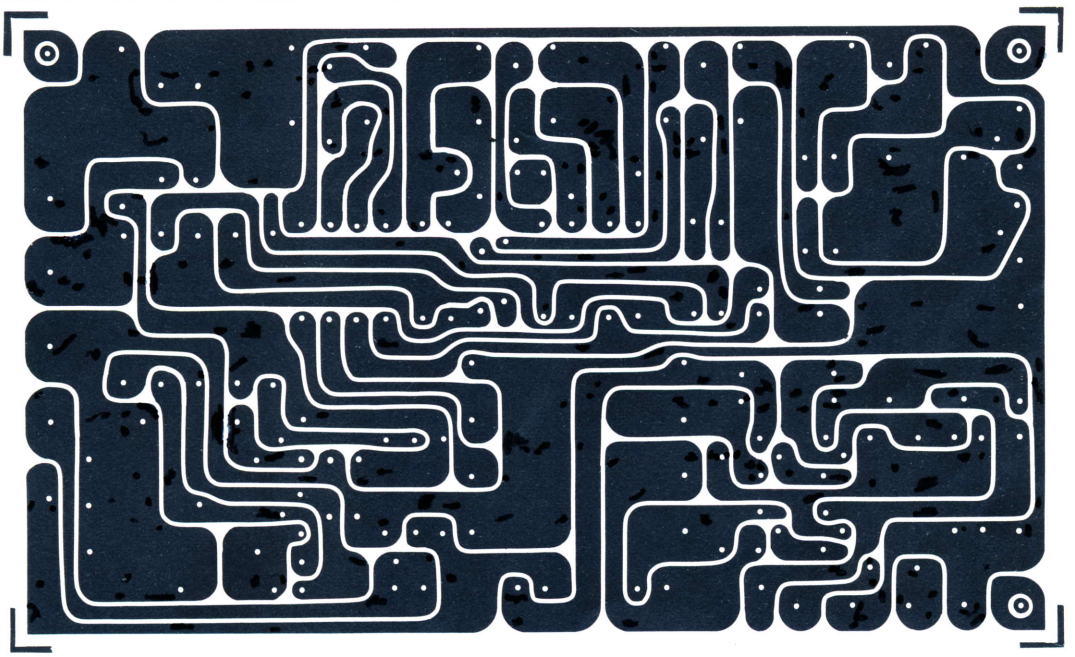
Resistors:
R1 = 2M7
R2 = 4M7
R3,R4,R5,R12 = 1 k
R6,R9,R13 = 4k7
R7 = 39 k
R8 = 5k6
R10 = 47 k
R11 = 220 k
R14 = 100 k
R24 = 470 Ω

Capacitors:
C1 = 1 μ, 6 V tantalum
C2 = 470 μ, 6 V
C3 = 100 μ, 16 V
C4 = 100 μ, 25 V
C5,C6 = 2n2
C7 = 39 n
C8,C9,C12 = 25 μ, 16 V
C10 = 1 n
C11 = 50 μ, 6 V

Semiconductors:
T1,T3 = TUN
T2 = TUP

Miscellaneous:
P1 = preset potentiometer 1 k lin.
P2 = potentiometer 4k7 log. stereo
P3,P4 = potentiometer 100 k lin. stereo
P5 = potentiometer 10 k lin.

6



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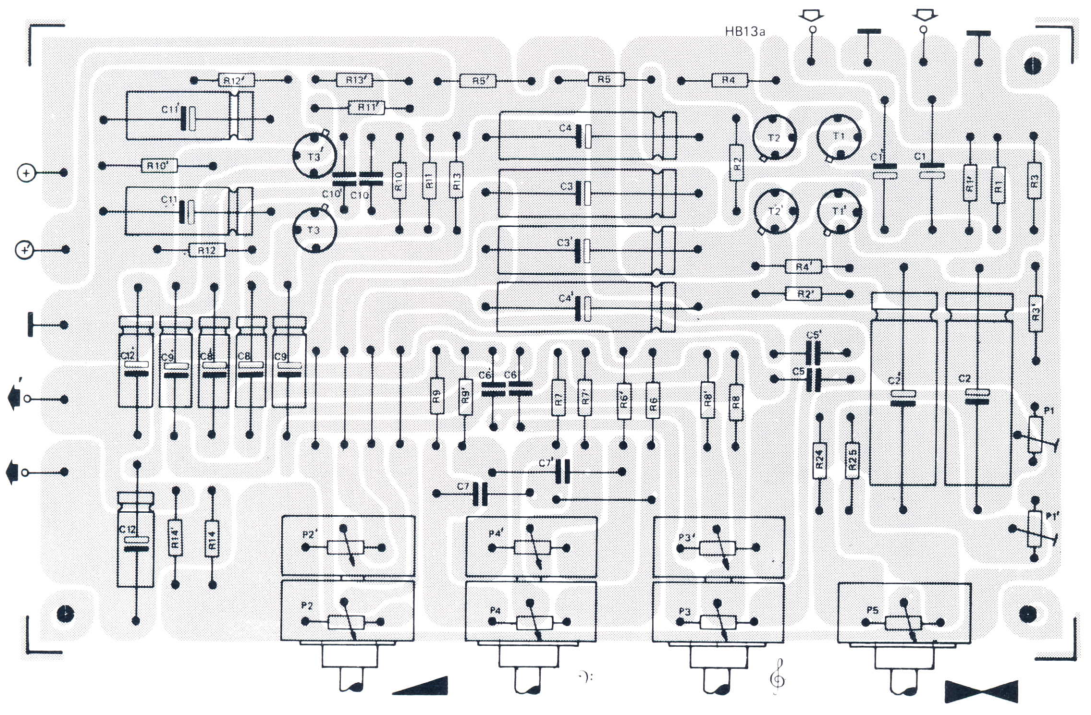

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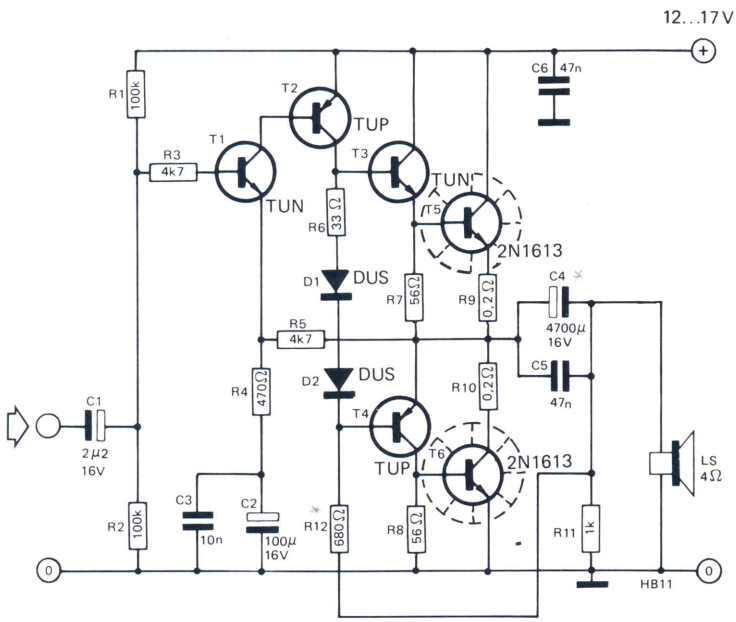

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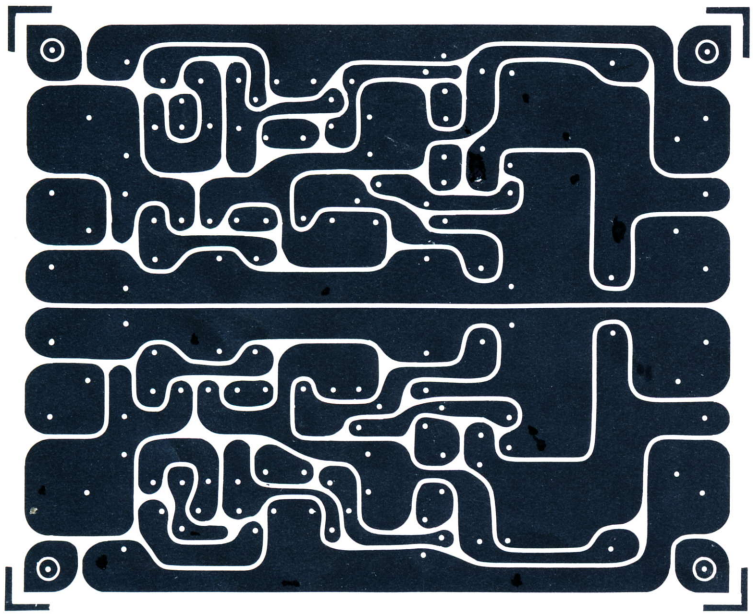

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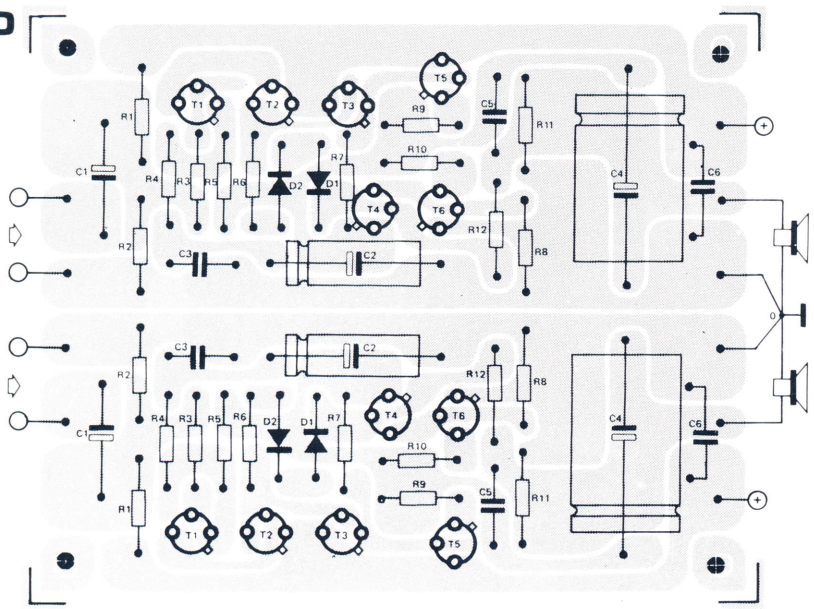


Figure 8. The output amplifier, which will deliver 3 watts into 4 Ω with a 12 volt supply and 3 watts into 8 Ω with a 17 volt supply. The different values for R12 and C4 are given in the table.

Figure 9. The printed circuit for the power amplifier is also symmetrical. It may be cut in half for mono applications if desired.

Figure 10. Component layout for the power amplifier p.c. board. (EPS HB11).

Figure 11. The circuit of the simple stabilised supply. The values of R1 and Z1 depend on the supply voltage required.

Figure 12. Board and component layout for the power supply. (EPS HB12).

Parts list for figures 8 and 10:

Resistors:
R1,R2 = 100 k
R3,R5 = 4k7
R4 = 470 Ω
R6 = 33 Ω
R7,R8 = 56 Ω
R9,R10 = 0,2 Ω
R11 = 1 k
R12 = see table

Capacitors:
C1 = 2,2 μ, 16 V
C2 = 100 μ, 16 V
C3 = 10 n
C4 = see table
C5,C6 = 47 n

Semiconductors:
T1,T3 = TUN
T2,T4 = TUP
T5,T6 = 2N1613
D1,D2 = DUS
2 TO5 heatsinks for T5 and T6

	12 V	17 V
R12	680 Ω	1 k
C4	4700 μ	2200 μ
LS	4 Ω	8 Ω

may be increased by reducing R4 but this is not recommended as instability may occur and in any case the overall gain of the system may be altered by adjusting P1 on the control amplifier board. The printed circuit for the power amplifier is given in figure 9 and the component layout in figure 10.

Supply

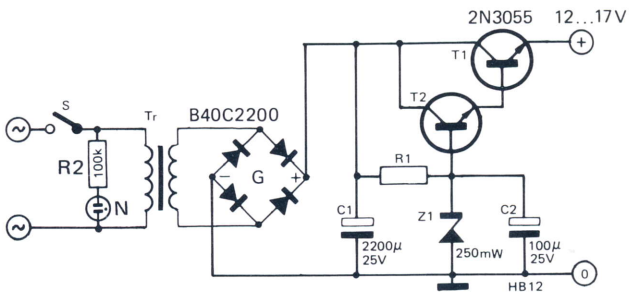
The regulated power supply is very simple, as can be seen from figure 11. T1 and T2 form a Darlington pair acting as a compound emitter-follower with a reference voltage provided by Z1. Z1 is chosen as a 13 or 18 volt zener for a 12 or 17 volt supply respectively. Since T2 dissipates only a small amount of power a heatsink is not required.
Figure 12 shows the board and component layout of the power supply. The component values for both versions are given in the table of figure 11.

Layout

The following layout precautions should be noted when assembling the completed board onto a chassis:

1. Loudspeaker common must be connected directly to the power supply common and should be kept well away from the boards.
2. Separate leads must be run from the supply to the supply points on each board.
3. Outputs of any board should be kept well away from inputs of other boards (except of course where the output of a stage is connected to the input of the succeeding stage).
4. Care should be taken to avoid earth loops. Each section of the amplifier should have only one connection to supply common.

11



Parts list for figures 11 and 12:

Resistor:
R1 = see table
R2 = 100 k

Capacitors:
C1 = 2200 µ, 25 V
C2 = 100 µ, 25 V

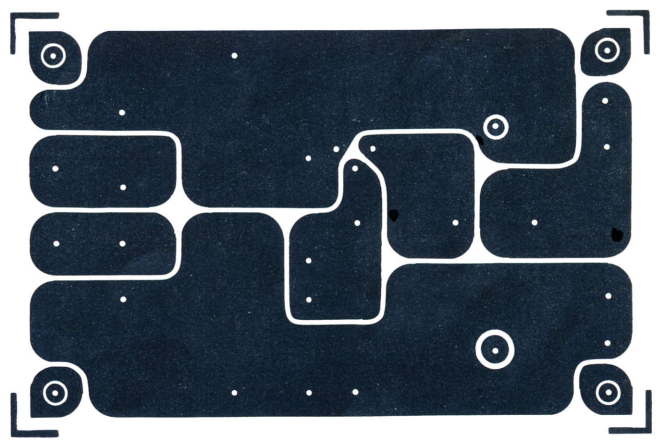
Semiconductors:
T1 = 2N3055
T2 = see table

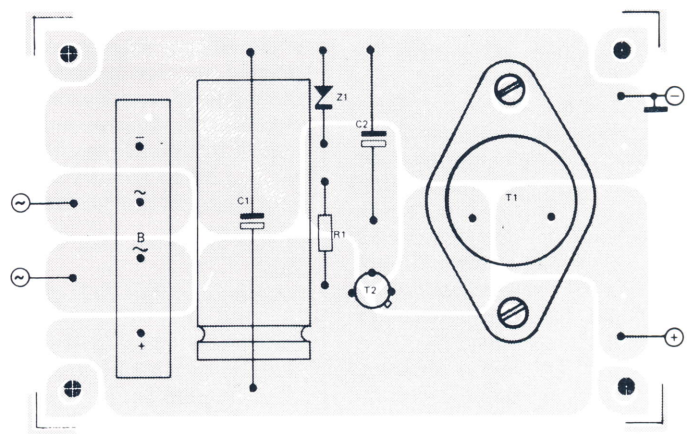
Transformer:
Tr1 = 2 A sec. see table

Miscellaneous:
G = B40C2200 40 V 2.2 A bridge rec.
or 4 x 1N4001
Z1 = zener diode, 250 mW, see table
N = neon
S = switch on/off

	12 V	17 V
R1	270 Ω	680 Ω
Z1	13 V	18 V
T2	TUN	BC 107
Tr	12 V ~	18 V ~

12





tup-tun-dug-dus

Wherever possible in Elektor circuits, transistors and diodes are simply marked 'TUP', 'TUN', 'DUG' or 'DUS'. This indicates that a large group of similar devices can be used without detriment to the performance of the circuit.

As far as possible, the circuits in Elektor are designed so that they can be built with standard components that most retailers will have in stock.
It is well-known that there are many general purpose diodes and low frequency transistors with different type numbers but very similar technical specifications. The difference between the various types is often little more than their shape. This family of semiconductors is referred to in the various articles by the following abbreviations:
TUP = Transistor, Universal PNP,
TUN = Transistor, Universal NPN,
DUG = Diode, Universal Germanium,
DUS = Diode, Universal Silicon.
TUP, TUN, DUG and DUS have to meet certain minimum specifications – they are not just 'any old transistor' or 'any old germanium diode'. . . .The minimum specifications are listed in tables 1a and 1b. It is always possible, of course, to use a transistor with better specifications than those listed!

Specifications and equivalents

A number of transistor types that meet the TUN specifications are listed in table 2. This list is, of course, incomplete – there are many more possible types.
Table 3 lists a number of possibilities for use as TUP, while table 4 gives equivalents for DUG and DUS.
A further group of better quality transistors are the BC107 - BC108 - BC109 (NPN) and BC177 - BC178 - BC179 (PNP) families. The minimum specifications are listed in table 5, while table 6 gives a list of equivalents. As will be obvious from the specifications, the main differences between the types are that the BC107/BC177 are higher voltage types (V_{ceo} = 45 volts) and the BC 109/BC179 are low-noise. If these differences are not important in a particular circuit, the various types are interchangeable.
The code letters A, B or C after the type number on these transistors denote various current amplification factors. For the A-types this is from 125 to 260, for the B-types it is 240 to 500 and for the C-types 450 to 900. A BC109C is therefore not a direct equivalent for a BC109B, for instance, although in many practical circuits it will make little or no difference.
When using the equivalent types BC167, -168, -169, BC257, -258, -259 or BC467, -468, -469 it should be noted that the base, emitter and collector leads are in a different order (see table 6).

elektor shorthand

From various enquiries it has become clear that some of our readers feel that they have been plunged in at the deep end. Elektor's 'shorthand' style of symbols and conventions seems to have led to some confusion, in spite of our efforts to the contrary, so some further explanation seems to be called for.

Resistor and capacitor codes

When giving the values of resistors and capacitors, decimal points and large numbers of zeros are avoided as far as possible. To this end, extensive use is made of the international abbreviations:

p (pico-)	= 10^{-12}	=	one millionth of one millionth;
n (nano-)	= 10^{-9}	=	one thousandth of one millionth;
μ (micro-)	= 10^{-6}	=	one millionth;
m (milli-)	= 10^{-3}	=	one thousandth;
E	= 10^{0}	=	unity;
k (kilo-)	= 10^{3}	=	one thousand times;
M (mega-)	= 10^{6}	=	one million times;
G (giga-)	= 10^{9}	=	one thousand million times;

Furthermore, the symbols Ω (ohm) and F (farad) are usually omitted, since it is normal practice to state resistance values in ohms and capacitance values in farads. Finally, the decimal point is usually replaced by one of the abbreviations (p, n, μ . . .) listed above (This has also been accepted practice for some years).

A few examples may serve to clarify all this:
Resistance value 2k7: this is 2.7 kΩ, or 2700 Ω.
Resistance value 470: this is 470 Ω.
Resistance value 3M9: this is 3.9 MΩ, or 3,900,000 Ω.
Capacitance value 4p7: this is 4.7 pF, or 0.000 000 000 004 7 F . . .
Capacitance value 100 μ: this is 100 μF.
Capacitance value 4700 μ: this is 4700 μF, and could have been written as 4m7 – but never is.
Capacitance value 10 n: this is 10 nF, and is also sometimes written (but not in elektor!) as 10,000 pF or 0.01 μF; or even as 10 kpF (10 kilo-pico-Farad), which is a horrible confusion of symbols. In the same way one sometimes finds $\mu\mu$F (micro-micro-Farad) instead of pF.

Semiconductor type numbers

Very often, a large number of equivalent types for one integrated circuit exist with different type numbers. On closer examination, a group of digits are often found to be identical, but they are pre- or suffixed with letters and digits which denote the manufacturer. As an example, a popular op-amp is variously denoted as μA741, LM741, L741, MC1741, MIC741, RM741, SN72741 or ZLD741, to name a few. To cut through this confusion, this IC is referred to in elektor as a '741' – which means that we couldn't care less who makes it, provided it meets the specifications. . .

TUP TUN DUG DUS

	type	U_{ceo} max	I_c max	h_{fe} min.	P_{tot} max	f_T min.
TUN	NPN	20 V	100 mA	100	100 mW	100 MHz
TUP	PNP	20 V	100 mA	100	100 mW	100 MHz

Table 1a. Minimum specifications for TUP and TUN.

Table 1b. Minimum specifications for DUS and DUG.

	type	U_R max	I_F max	I_R max	P_{tot} max	C_D max
DUS	Si	25 V	100 mA	1 μA	250 mW	5 pF
DUG	Ge	20 V	35 mA	100 μA	250 mW	10 pF

Table 2. Various transistor types that meet the TUN specifications.

TUN		
BC 107	BC 208	BC 384
BC 108	BC 209	BC 407
BC 109	BC 237	BC 408
BC 147	BC 238	BC 409
BC 148	BC 239	BC 413
BC 149	BC 317	BC 414
BC 171	BC 318	BC 547
BC 172	BC 319	BC 548
BC 173	BC 347	BC 549
BC 182	BC 348	BC 582
BC 183	BC 349	BC 583
BC 184	BC 382	BC 584
BC 207	BC 383	

Table 3. Various transistor types that meet the TUP specifications.

TUP		
BC 157	BC 253	BC 352
BC 158	BC 261	BC 415
BC 177	BC 262	BC 416
BC 178	BC 263	BC 417
BC 204	BC 307	BC 418
BC 205	BC 308	BC 419
BC 206	BC 309	BC 512
BC 212	BC 320	BC 513
BC 213	BC 321	BC 514
BC 214	BC 322	BC 557
BC 251	BC 350	BC 558
BC 252	BC 351	BC 559

Table 4. Various diodes that meet the DUS or DUG specifications.

DUS		DUG
BA 127	BA 318	OA 85
BA 217	BAX13	OA 91
BA 218	BAY61	OA 95
BA 221	1N914	AA 116
BA 222	1N4148	
BA 317		

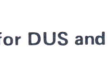
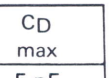
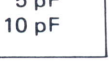
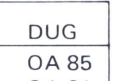
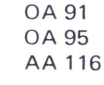
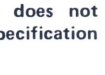
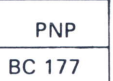
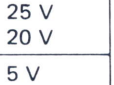
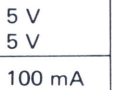
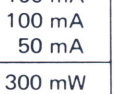
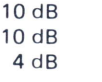
Table 5. Minimum specifications for the BC107, -108, -109 and BC177, -178, -179 families (according to the Pro-Electron standard). Note that the BC179 does not necessarily meet the TUP specification ($I_{c,max}$ = 50 mA).

	NPN	PNP
	BC 107 BC 108 BC 109	BC 177 BC 178 BC 179
V_{ce_0} max	45 V 20 V 20 V	45 V 25 V 20 V
V_{eb_0} max	6 V 5 V 5 V	5 V 5 V 5 V
I_c max	100 mA 100 mA 100 mA	100 mA 100 mA 50 mA
$P_{tot.}$ max	300 mW 300 mW 300 mW	300 mW 300 mW 300 mW
f_T min.	150 MHz 150 MHz 150 MHz	130 MHz 130 MHz 130 MHz
F max	10 dB 10 dB 4 dB	10 dB 10 dB 4 dB

The letters after the type number denote the current gain:

A: a' (β, h_{fe}) = 125-260
B: a' = 240-500
C: a' = 450-900.

Table 6. Various equivalents for the BC107, -108, . . . families. The data are those given by the Pro-Electron standard; individual manufacturers will sometimes give better specifications for their own products.

NPN	PNP	Case	Remarks
BC 107 BC 108 BC 109	BC 177 BC 178 BC 179		
BC 147 BC 148 BC 149	BC 157 BC 158 BC 159		P_{max} = 250 mW
BC 207 BC 208 BC 209	BC 204 BC 205 BC 206		
BC 237 BC 238 BC 239	BC 307 BC 308 BC 309		
BC 317 BC 318 BC 319	BC 320 BC 321 BC 322		I_{cmax} = 150 mA
BC 347 BC 348 BC 349	BC 350 BC 351 BC 352		
BC 407 BC 408 BC 409	BC 417 BC 418 BC 419		P_{max} = 250 mW
BC 547 BC 548 BC 549	BC 557 BC 558 BC 559		P_{max} = 500 mW
BC 167 BC 168 BC 169	BC 257 BC 258 BC 259		169/259 I_{cmax} = 50 mA
BC 171 BC 172 BC 173	BC 251 BC 252 BC 253		251 . . . 253 low noise
BC 182 BC 183 BC 184	BC 212 BC 213 BC 214		I_{cmax} = 200 mA
BC 582 BC 583 BC 584	BC 512 BC 513 BC 514		I_{cmax} = 200 mA
BC 414 BC 414 BC 414	BC 416 BC 416 BC 416		low noise
BC 413 BC 413	BC 415 BC 415		low noise
BC 382 BC 383 BC 384			
BC 437 BC 438 BC 439			P_{max} = 220 mW
BC 467 BC 468 BC 469			P_{max} = 220 mW
	BC 261 BC 262 BC 263		low noise

TUP TUN DUG DUS

tup tun tester

This tester gives an instant check of the 'general health' of a transistor, as well as its compliance with the minimum TUP or TUN specification, by the very simple procedure of plugging it into test sockets and interpreting the messages from two light-emitting diodes. It is also possible to check diodes for excessive capacity or leakage.

The principle of operation is simple and no preliminary calibration is needed – only the use of transistors and diodes known to be 'good' and resistors within the specified tolerance.

An astable multivibrator generates a square wave at a frequency of about 2 kHz, and this oscillation is turned on and off by another multivibrator at about 2 Hz. The collector-emitter path of the transistor under test (or the anode-cathode path of the diode) is connected in series with another transistor across the supply rails, and the intermittent 2 kHz square wave is fed in antiphase to the bases of each of the two transistors. Figure 1 shows a block diagram of the arrangement, from which a lot of information about the semiconductor under test can be deduced from the 'behaviour', voltage-wise, of the junction between the two semiconductors. This information can be displayed with the aid of only two light-emitting diodes (LEDs).

Circuit Description

Figure 2 shows the complete circuit, which has been divided into three sections to avoid confusion. Transistors T5 and T6 in figure 2a form an astable multivibrator which runs at about 2 kHz. T2 and T3 form another multivibrator which runs at a much lower speed, about 2 Hz, and turns the 'fast' (2 kHz) oscillator on and off through transistor T4, which also supplies a 2 Hz switching waveform, via connection 'Q', to the display section T7 ... T9 and LEDs 'A' and 'B' (figure 2c). A similar 2 Hz switching waveform, in antiphase to the one which appears at 'Q', is supplied to the display section by T1 via 'P'. As will be seen later, these switching waveforms are needed to enable an unambiguous display to be obtained from two LEDs only.

An optional third LED (shown in the circuit as LED 'C') can be connected in series with the 680 Ω resistor R9 between 'Q' and supply negative. This will give a partial test of the tester itself by blinking in step with the slow oscillator if this is functioning.

2 kHz square waves of equal amplitude and opposite polarity are produced intermittently at the collectors of T5 and T6. These two points, which drive the whole of the test circuitry, are marked 'X' and 'Y' respectively. When the fast oscillator is turned off, T5 is cut off and its collector ('X') is at its higher potential.

The left-hand half of figure 2b is the section in which PNP-transistors are tested. It has been shown that 2 kHz square waves of equal amplitude and opposite polarity are being injected intermittently at 'X' and 'Y'.

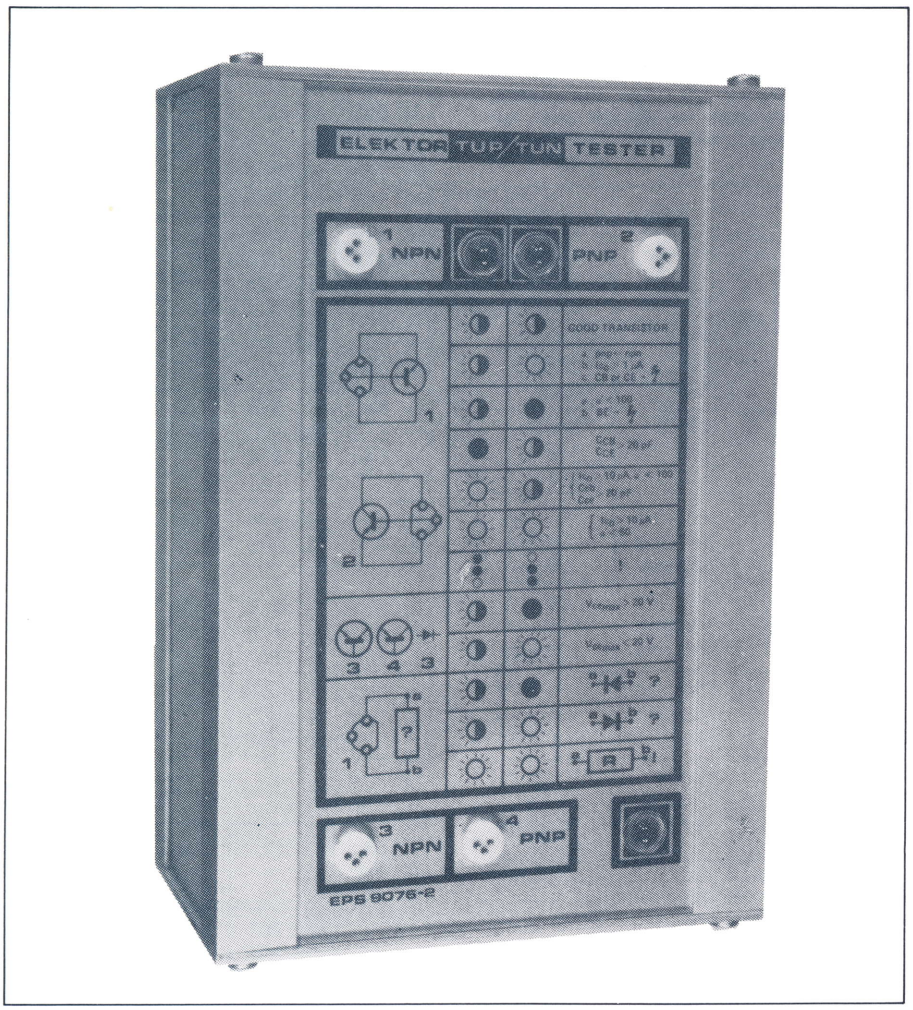
Display

Assume that a (good) PNP transistor is plugged in at the test point T_A in figure 2b. When the fast oscillator is off, 'X' is positive and 'Y' is negative. (The terms 'positive' and 'negative' are used to denote the higher and lower potentials taken up by various points in the circuit). Both the transistor T10 and the transistor T_A under test are therefore cut off, and the connection joining the collectors of T10 and T_A is floating. The diode D10 does not pass any current and the Darlington pair T11 and T12 is cut off. Figures 2b and 2c show that the collector of T12 is one of the points connected to the base of T9 (point A). When T12 is cut off, 'A' is positive and T9 is therefore also cut off. LED 'B', which is in the collector lead of T9, is therefore off, and the collector of T9 is negative.

To find what LED 'A' is doing, the other switching waveforms, derived from the slow oscillator via 'P' and 'Q', must now be examined. To switch the fast oscillator off, 'Q' must be negative; therefore 'P' is positive. T7 is connected to 'P', so T7 can conduct if its base receives a positive drive from the collector of T9 via R19.

In the situation now under consideration, however, the collector of T9 is negative and T7 does not pass current. T8 is also returned to the negative rail through LED 'A', but 'Q' is negative so LED 'A' stays off.

Recapping at this stage; with a good



transistor and when the fast oscillator is turned off, both LEDs are off.

It has been seen that the three points which determine the LED display are 'A', 'P' and 'Q'. The basic relationship is as follows:

1. When 'P' is positive (i.e. the fast oscillator is turned off), LED 'A' will light up if the base of NPN transistor T7 is driven positively from the collector of T9.
2. When 'Q' is positive (i.e. the fast oscillator is turned on), LED 'A' will light up if the base of PNP transistor T8 is driven negatively from the collector of T9.
3. LED 'B' lights up when the collector of T9 is positive, irrespective of whether 'P' or 'Q' is positive.
4. When 'A' is negative, the collector of T9 is positive.

These relationships can be combined in a kind of truth table which will help in predicting the display for transistors or diodes in different states of health. They are also summarised, in a slightly different form, in figure 3a + b.

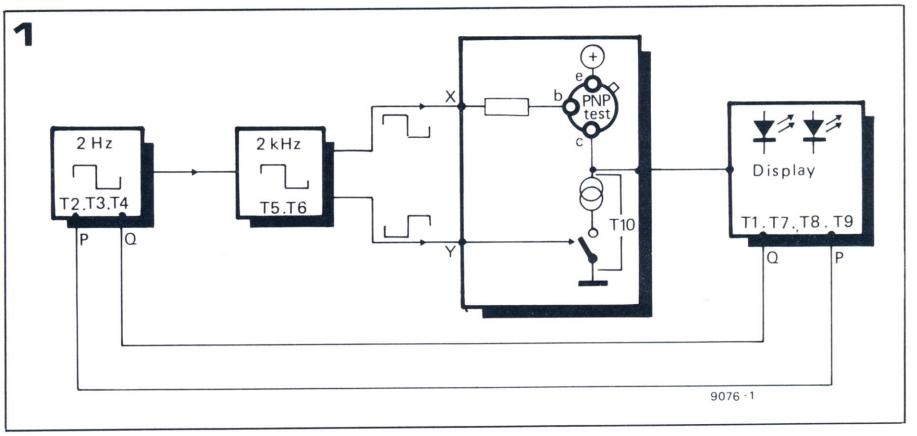
FAST OSCILLATOR TURNED	'A' SWINGS	LED A	LED B
Off	positive	Off	Off
Off	negative	On	On
On	positive	On	Off
On	negative	Off	On

What happens during the bursts when the fast oscillator is turned on?

'X' and 'Y' are being swung alternately positive and negative with opposite polarities at 2 kHz. When 'X' swings positive and 'Y' swings negative, the same reasoning which was applied to the situation when the fast oscillator is turned off will indicate that 'A' swings positive and LED 'B' is off. In this case, however, the fast oscillator is turned on ('Q' is therefore positive) and LED 'A' lights up.

When 'X' swings negative and 'Y' swings positive, it will be seen from figure 2b that both T10 and the transistor under test in T_A are turned on. The emitter of T_A is directly connected to supply positive, while the emitter of T10 is connected to supply negative through the 470 Ω resistor R28. If the current gain of T_A is high enough, the potential at the collector of T_A will move positively, D10 will conduct and the base of T11 will also move positively. (This will be discussed in more detail later.) The emitter of T12, the other transistor in the Darlington pair, is held by R30 and R31 at half the supply rail potential, so T12 is turned on; its collector potential (point 'A') swings negative and, as can be seen from the table, LED 'B' lights up and LED 'A' is off.

So the LED display while the fast oscillator is turned on and the transistor is a 'good' one is that 'A' and 'B' each come on during alternate half-cycles of the 2 kHz oscillation. Both LEDs therefore appear to be on during each 2 kHz burst, and it has already been seen that both are off while the fast oscillation is turned off.



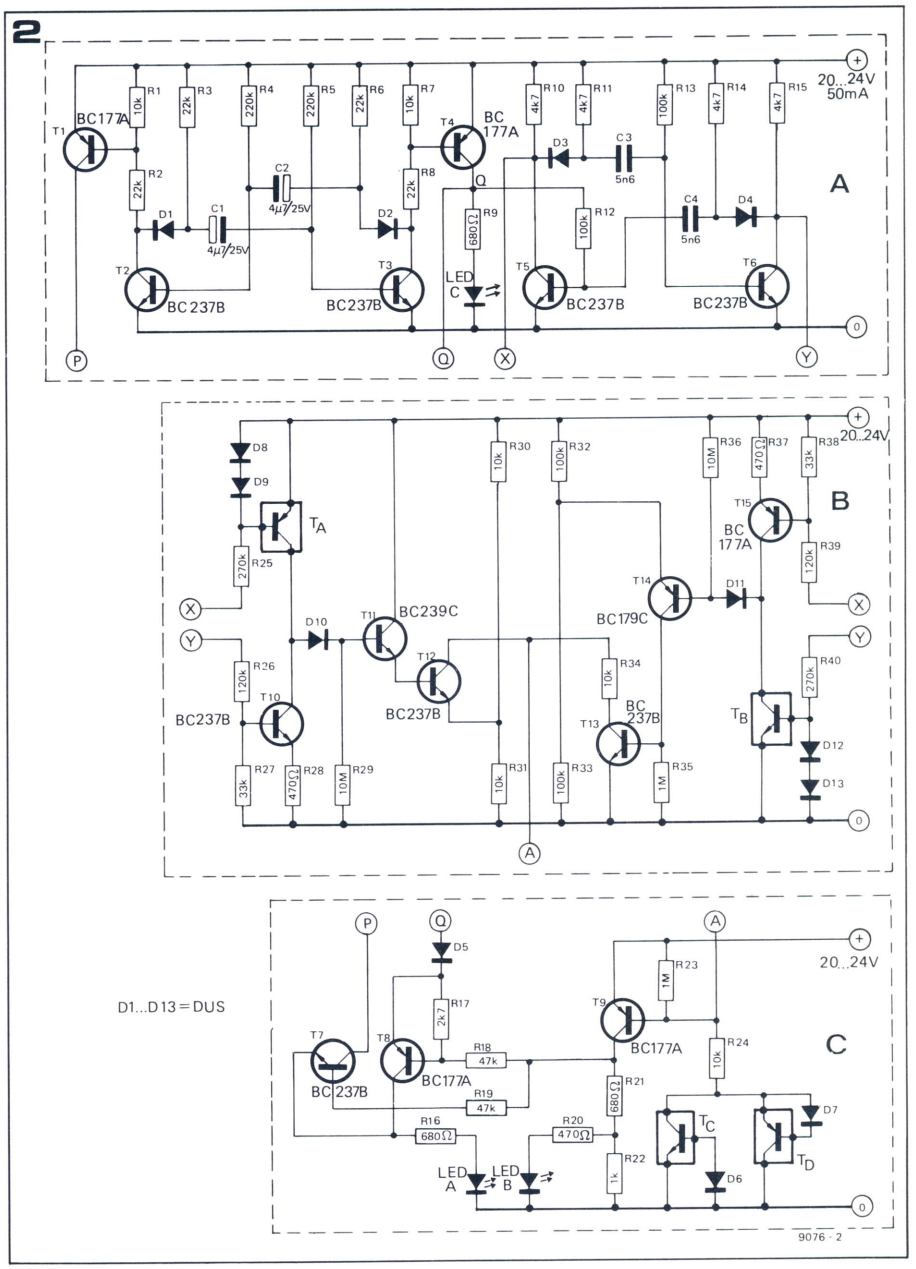


Figure 1. Block diagram of the arrangement for testing a PNP transistor. For clarity, the breakdown voltage test and the complementary test for an NPN transistor have been omitted.

Figure 2. Complete circuit of the TUP/TUN tester. Block A is the collector section, B contains the test bridges for NPN and PNP transistors and C shows the breakdown voltage testing and display sections.

The full display cycle for a 'good' transistor is that both LEDs blink on and off together (figure 3c). It will be seen later that this display occurs only with a transistor which is good according to all the criteria that are tested in socket T_A.

Transistor with low current gain (α')

When the fast oscillator is turned off,

'X' swings positive and 'Y' swings negative, so both T10 and the transistor under test in T_A are cut off. Their commoned collectors are floating, and by the same sequence of events as described for a good transistor, the voltage at the collector of T9 is low and LED 'B' is off. It can be deduced from the table that this combination of switching voltages leads to LED 'A' also being off.

When the fast oscillator comes on and swings 'X' and 'Y' negative and positive respectively, T10 and T_A are both turned on. The potential at the base of T10 is therefore determined by the potentiometer R15 (figure 1a), R26 and R27, i.e.

$$20 \times \frac{33}{4.7 + 120 + 33} = 4.2 \text{ V}.$$

The base-emitter voltage drop in T10 will be about 0.7 V, so the voltage at the emitter of T10 cannot rise above 4.2 V – 0.7 V = 3.5 V. T10 is therefore acting as a current source, its collector current being stabilised at the value determined by this latter voltage and the emitter resistor R28, i.e.

$$\frac{3.5 \times 1000}{470} \text{mA} \approx 7.4 \text{ mA}$$

As the emitter of T_A is directly connected to the positive supply rail, its base current is determined by the voltage (about 19 V) between 'X' and the positive rail, and by R25, i.e.

$$\frac{18 \times 10^6}{270 \times 10^3} \mu\text{A} \approx 70 \mu\text{A}$$

(the base-emitter resistance can be disregarded in this context).

It has been mentioned that T10 acts as a current source attempting to stabilise the collector current through both transistors at 7.4 mA, which corresponds to a current gain of something over 100 for the transistor under test. If T_A cannot produce this current, T6 bottoms and the voltage at the connected collectors of T_A and T10 becomes too low for T11 and T12 to be turned on (figure 3d). So the potential at 'A' remains positive and LED 'B' stays off. The table will show that LED 'A' comes on.

When the fast oscillator swings to its other polarity (i.e. 'X' swings positive and 'Y' swings negative) the linked collectors of T_A and T10 revert to the floating condition, so that the Darlington pair T11 and T12 remains non-conductive and 'A' positive. LED 'B' therefore stays off and LED 'A' stays on.

Summarising: the LED display with a transistor of low current gain is that LED 'A' blinks and LED 'B' stays on.

Transistor with high capacitances

When the fast oscillator is turned off, the situation is the same as in both the cases already examined: T10 and the transistor under test are both cut off, and this leads to LED 'A' and LED 'B' both being off. When the fast oscillator comes on and swings 'X' negatively and 'Y' positively, both transistors are turned on, but if T_A has high collector-to-base (C_{cb}) and/or collector-to-emitter (C_{ce}) capacitance, its response is delayed. The voltage rise at its collector is slowed down as these capacitances discharge, but the voltage will probably level off at its 'final' value before the end of the period in which T_A is turned on, and when this happens LED 'B' comes on while LED 'A' stays off (figure 3e).

When, however, T_A and T10 are once more turned off by the swings at 'X' and 'Y', the capacitances can recharge only through the Darlington pair T11 and T12 (which has, by definition, a high input impedance) and through the 10 MΩ resistor R29. The drop in potential at the collector of T_A, as the capacitances recharge, is slower than it would be with a normal transistor, and if the capacitances are too large the potential will not fall far enough to turn T11 off (and therefore LED 'A' on and LED 'B' off) before the time when T_A and T10 are turned on once again. So LED 'B' will stay on, and LED 'A' off, throughout each period when the fast oscillator is turned on.

With slightly smaller capacitances, LED 'A' may come on dimly if the slow recharge of excess capacitance only allows this LED to turn on for a small

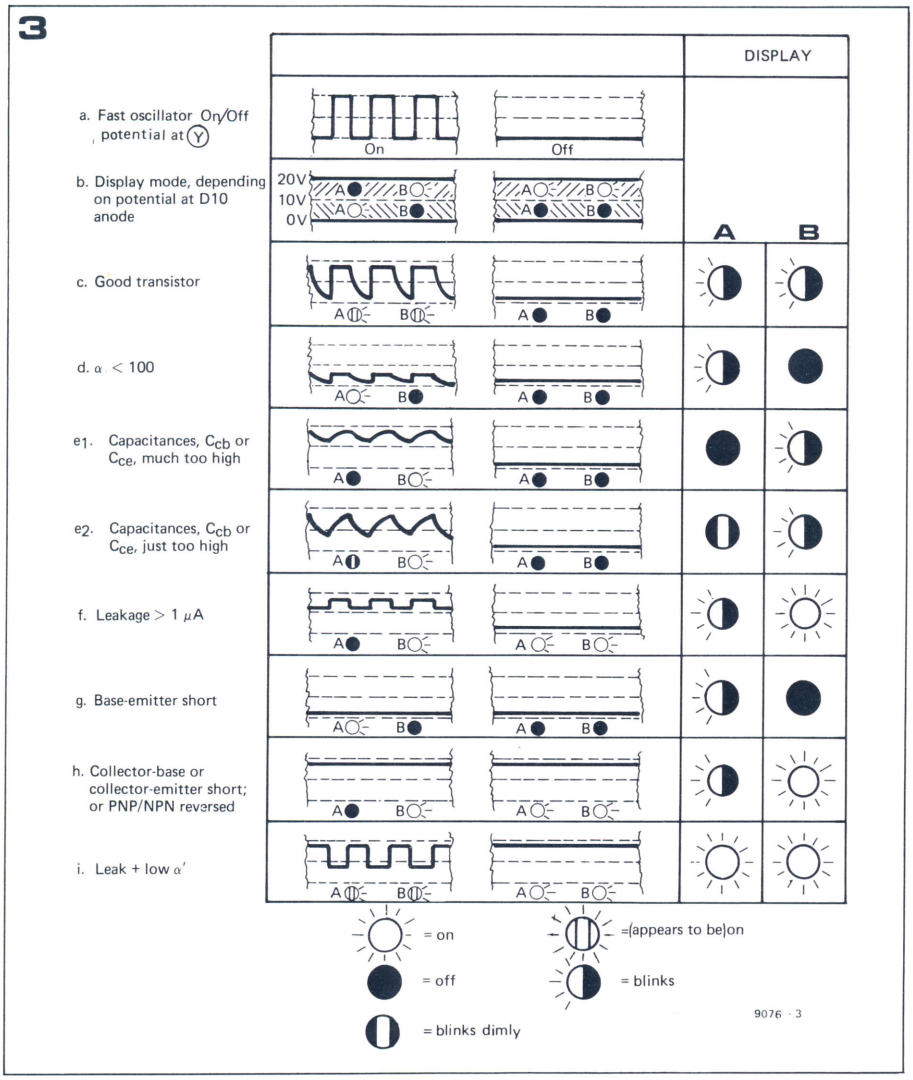


Figure 3. Summary of LED displays, based on the waveforms at the collector of the transistor under test.

Figure 4. Transistor testing chart, showing what the various displays signify. This chart is derived from figure 3.

Figure 5. Transistor (or diode) breakdown test chart.

Figure 6. The conduction test for diodes, in the 'PNP' test socket, is shown in figure 6A. The leakage test for diodes is shown in figure 6B.

Figure 7. Tests to test the tester.

4

DISPLAY LED A	DISPLAY LED B	MEANING
◑	◑	Good transistor
◑	☀	a. PNP/NPN reversed b. Leak > 1 μA c. C-B short d. C-E short
◑	●	a. α′ < 100 b. B-E short
●	◑	C-B or C-E capacitance > 20p
☀	◑	Leak > 10 μA + very low α′ + large C_{cb} or C_{ce}
◐	◑	C_{cb} or C_{ce} ≈ 20p
☀	☀	Leak > 10 μA + α′ < 50
●	●	Impossible. If this happens something is wrong with the tester. Check the power supply!

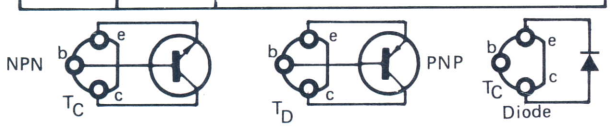
☀ = On continuously ◑ = Blinks

◐ = Blinks dimly ● = Off

9076-4

5

DISPLAY LED A	DISPLAY LED B	MEANING
◑	●	Good (Breakdown voltage > 20 V)
◑	☀	Fail (or connections reversed)



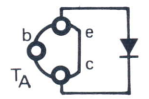
Key to display as for figure 4.

9076-5

6 a

DISPLAY LED A	DISPLAY LED B	MEANING
◑	☀	Conducts satisfactorily
◑	●	Not conducting, i.e. open circuit or connections reversed

Key to display as for figure 4.

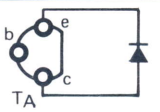


9076-6A

b

DISPLAY LED A	DISPLAY LED B	MEANING
◑	●	Blocks satisfactorily
◑	☀	a. Leaks severely b. Shorted c. Connections reversed
☀	☀	Leaks

Key to display as for figure 4



9076-6B

7

TEST APPLIED	DISPLAY LED A	DISPLAY LED B
1. Nothing plugged into any test socket	◑	●
2. Base and collector or emitter and collector sockets shorted in T_A or T_B.	◑	☀
3. PNP or NPN transistor known to be good, correctly plugged into T_A or T_B as applicable	◑	◑
4. As previous test, but with a 22 p capacitor connected from collector to base or emitter	●	◑
5. Emitter and base leads of a PNP or NPN transistor known to be good connected to the collector and emitter sockets of T_C or T_D, whichever is appropriate; i.e. reverse-diode check of breakdown voltage testing section	◑	☀

Key to display as for figure 4

9076-7

part of each fast-oscillator cycle. Summarising again: the display for high capacitance is that LED 'B' blinks on and off while LED 'A' remains off or blinks dimly.

Transistor with high leakage

A transistor with high leakage current tends to behave, from the tester's point of view, as though it were turned on all the time. In all the cases examined so far, no collector current flows in the transistor under test while the fast oscillator is turned off. If, however, there is a leakage current between collector and emitter, this will flow through D10 and R29 to the negative rail even when 'X' is positive and both T_A and T10 are supposed to be cut off. This leakage current develops a voltage across the 10 MΩ resistor R29, and therefore raises the potential at the base of T11.

It will be recalled that the emitter of T12 is held at half the supply voltage (i.e. at about 10 volts) by the potentiometer R30 and R31. So if the leakage current is a little more than 1 μA, it will build up a voltage sufficient to turn on T11 and T12 and thus light up LED 'A' and LED 'B' while the fast oscillator is off. When the fast oscillator is turned on and the display transistors are switched through 'P' and 'Q', LED 'B' stays on but LED 'A' goes out (figure 3f). So with a transistor having a leakage current of 1 μA or more, LED 'B' stays on and LED 'A' flashes.

Transistor with base and collector or emitter and collector short-circuited

A transistor with one of these faults 'looks like' one with high leakage (only more so). A current can flow from the positive rail through the emitter-base

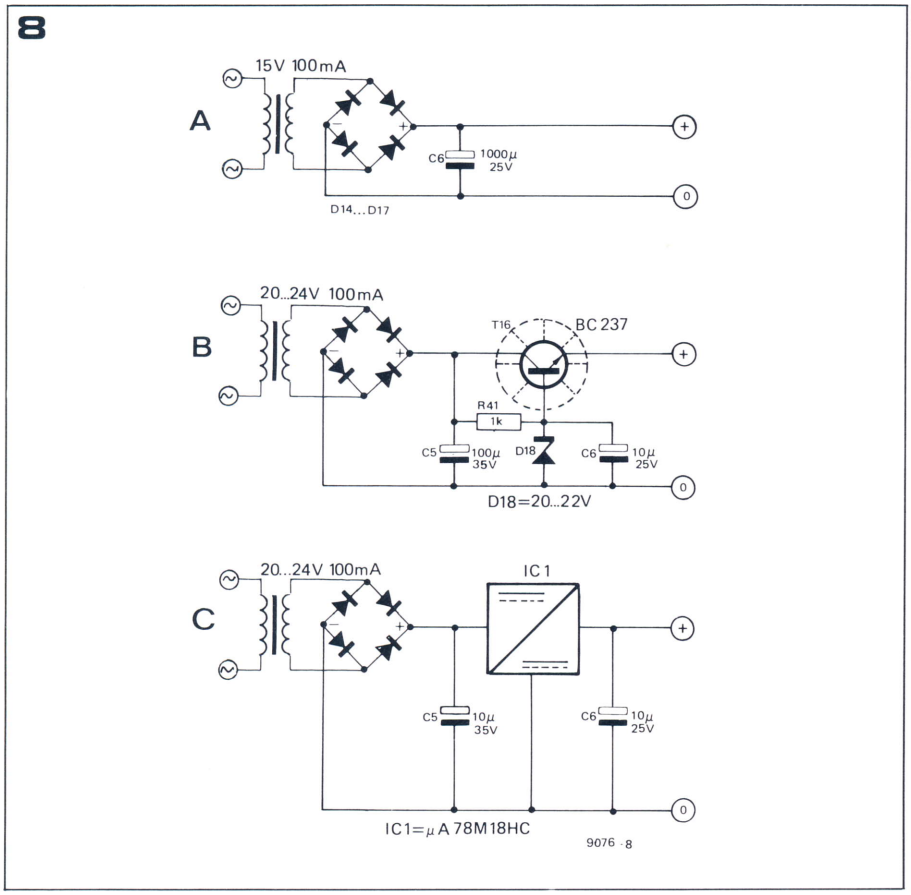


Figure 8. Alternative power supply arrangements, depending on the components one can obtain.

Figure 9. The p.c.b. and component layout for the TUP/TUN tester. Three alternative layouts are given, corresponding to the three power supply arrangements.

junction and the base-collector short in T_A (or directly through the emitter-collector short), through D10, and through the 10 MΩ-resistor R29. It has been shown that a leakage current as low as 1 µA can turn on T11 and T12 and therefore make LED 'B' light up and LED 'A' go out while the fast oscillator is on. When the fast oscillator is off, LED 'A' lights up and 'B' stays on. So the display with base and collector or emitter and collector short-circuited is that LED 'B' stays on all the time, and LED 'A' blinks on and off (figure 3h).

Transistor with base and emitter short-circuited

When the base and emitter are short-circuited, no 'normal' base current can flow, and therefore there is no collector current. So the transistor 'looks like' one with zero α', and the LED display is the same: i.e. LED 'A' blinks and LED 'B' stays off (figure 3g).

Combined leak and low current gain or combined leak and base-emitter short

While the fast oscillator is off, the display is the same as for a leaky transistor: both LED 'A' and LED 'B' are on. When the fast oscillator is on and is turning T_A and T10 off, the leakage current holds the collectors of T_A and T10 high enough in potential to turn on T11, resulting in LED 'A' being off and LED 'B' being on. When the fast oscillator turns T_A and T10 on, the low current gain of T_A allows T10 to 'overcome' both the leakage current and the collector current (if any) in T_A and pull down the potential of the commoned collectors, whereupon LED 'A' comes on and LED 'B' goes off. This alternate lighting up of LED 'A' and LED 'B' is at the speed of the fast oscillator, and both LEDs stay on while the fast oscillator is turned off, so we have a display cycle in which both LEDs appear to be on continuously (figure 3i).

Other combinations of Faults

It would not be a very profitable exercise to list the LED displays with all possible combinations of faults, but it can be said that only a transistor which is 'sound in wind and limb' according to all the test criteria will give the 'good transistor' display in both test sockets.

PNP and NPN transistors

The foregoing descriptions apply to PNP transistors. They also hold good, mutatis mutandis, for NPN transistors plugged into test socket T_B, which appears on the right-hand side of figure 2b. The functions performed by T10, T11 and T12 and associated components for PNP transistors are performed by T13, T14 and T15 and associated components for NPN transistors. In this case, however, the transistors T13 and T14 which pass on a voltage drop at the anode of D11 are not a Darlington pair but a complementary PNP-NPN-pair.

If a transistor is plugged into the wrong test socket (PNP into an NPN socket or vice versa), the base-to-collector path becomes equivalent to a forward-connected diode, and the display is the same as for a transistor with a base-collector short. The transistor will not be damaged, and it is clearly a good thing, when one shows up unexpectedly as 'faulty', to check whether it has been plugged into the wrong holes!

Breakdown Voltage Test

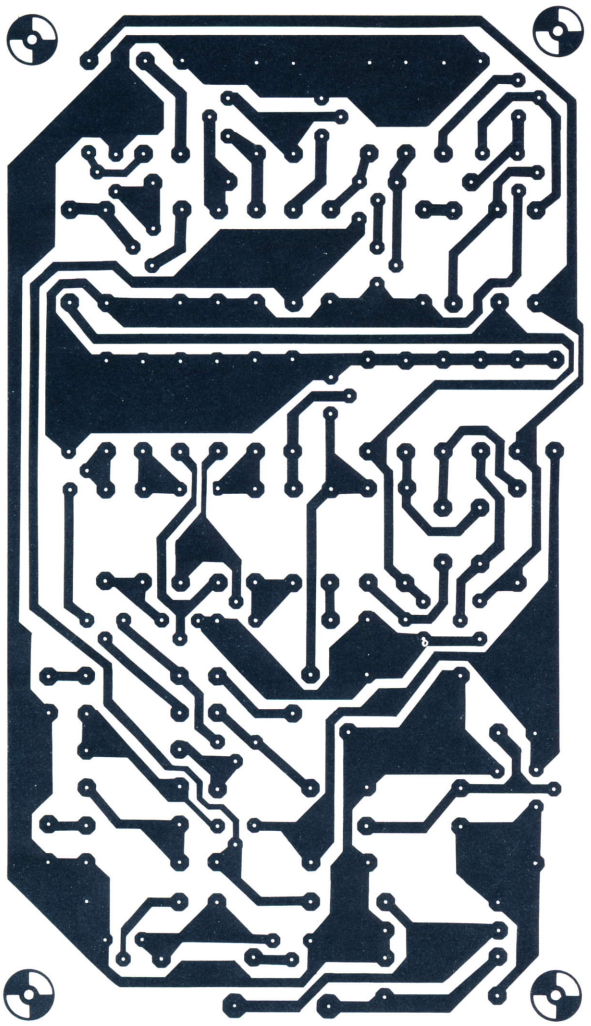
The sockets for this test are T_C and T_D, shown in figure 2c. The effective breakdown test voltage is about 20 V, and if a breakdown current flows the voltage at 'A' is pulled down continuously, resulting in LED 'A' blinking and LED 'B' staying on throughout the cycle. For a transistor which passes this test, LED 'A' blinks and LED 'B' stays off all the time (figure 5).

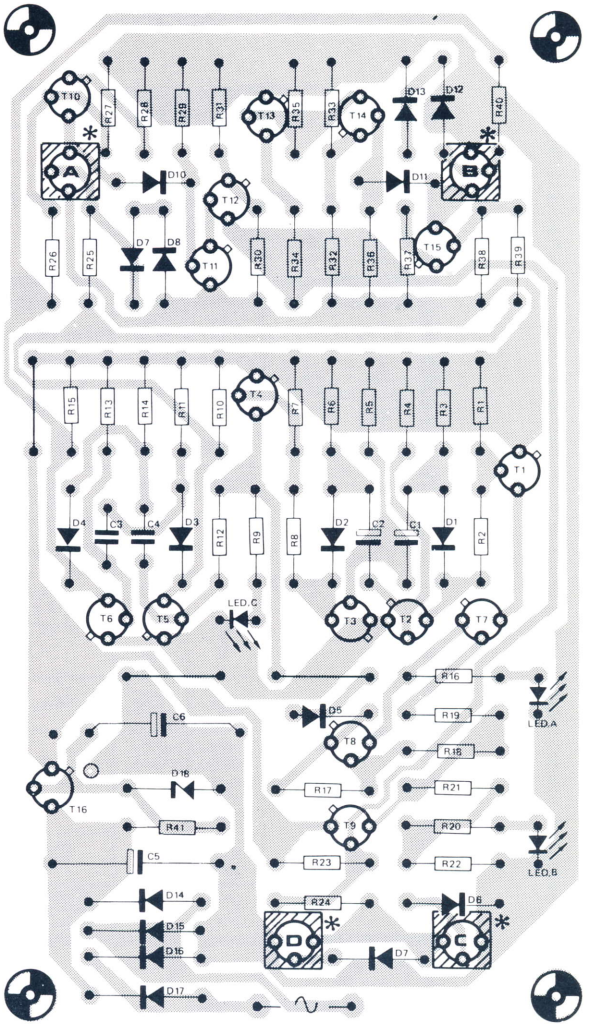
Diode Tests

By plugging the anode and cathode leads of a diode into the emitter and collector sockets of the PNP test points (or the other way round with the NPN test points) it can be tested for forward conduction, leakage and breakdown voltage. When the fast oscillator is off, the junction of the diode cathode and the collector of T10 will be held positive by the conduction of the diode, and if the conduction is good enough, this junction will remain positive when T10 is turned on (through 'Y') by the fast oscillator. When T10 is turned off the junction will still be positive. This leads to a display cycle in which LED 'A' blinks and LED 'B' stays on continuously (figure 6).

When the diode is non-conducting, open-circuited or connected the wrong way round, the junction of T10 collector and the cathode (or anode) will remain negative throughout the oscillator cycle, giving a LED display in which 'A' blinks and 'B' remains off. When a diode is deliberately connected the wrong way round, this display gives an indication (if the diode is a good one) that it is blocking properly in the reverse direction. If a diode is short-circuited or is leaking severely, it will give the same display, when plugged in the wrong way round, as a good diode connected the correct way round. It is just possible, however, that it *is* a good diode plugged

9



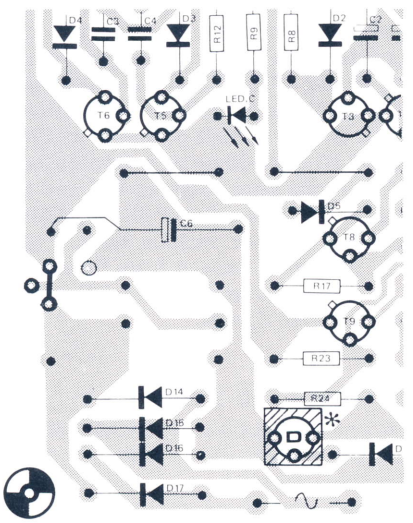


Stabilised supply with discrete components
Tr = 20 V/100 mA
R41 = 1 k
C5 = 100 µ/35 V
C6 = 10 µ/35 V
T16 = BC237B
D18 = 20 V Zener

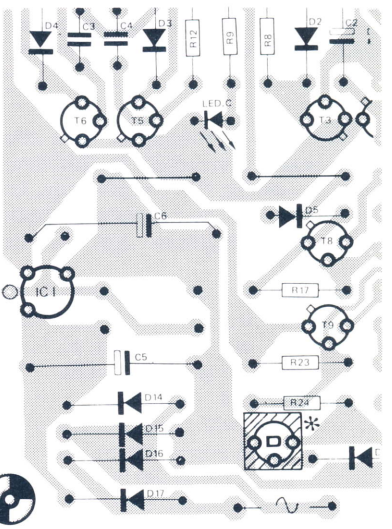
Parts list
Resistors:
R1,R7,R24,R30,R31,R34 = 10 k
R2,R3,R6,R8 = 22 k
R4,R5 = 220 k
R9 (if used),R16,R21 = 680 Ω
R10,R11,R14,R15 = 4k7
R12,R13,R32,R33 = 100 k
R17 = 2k7
R18,R19 = 47 k
R22 = 1 k
R25,R40 = 270 k
R26 = 120 k
R27,R38 = 33 k
R28,R37,R20 = 470 Ω
R29,R36 = 10 M
R23,R35 = 1 M
R39 = 120 k
R40 = 270 k

Capacitors:
C1,C2 = 4µ7
C3,C4 = 5n6

Semiconductors:
T1,T4,T8,T9,T15 = BC307B or equ.
T2,T3,T5,T6,T7,T10,T12,T13,T16 = BC237B or equ.
T11 = BC239C or equ.
T14 = BC179C or equ.
D1 ... D17 = BAX13, BY126, BY127, 1N4002, or other general-purpose silicon diodes
2 x LEDs



Unstabilised supply
Tr = 18 V/100 mA
C6 = 1000 µ/25 V



Stabilised supply with IC
Tr = 20 V/100 mA
C5 = 100 µ/35 V
C6 = 10 µ/35 V
IC = µA78M18HC or equ.

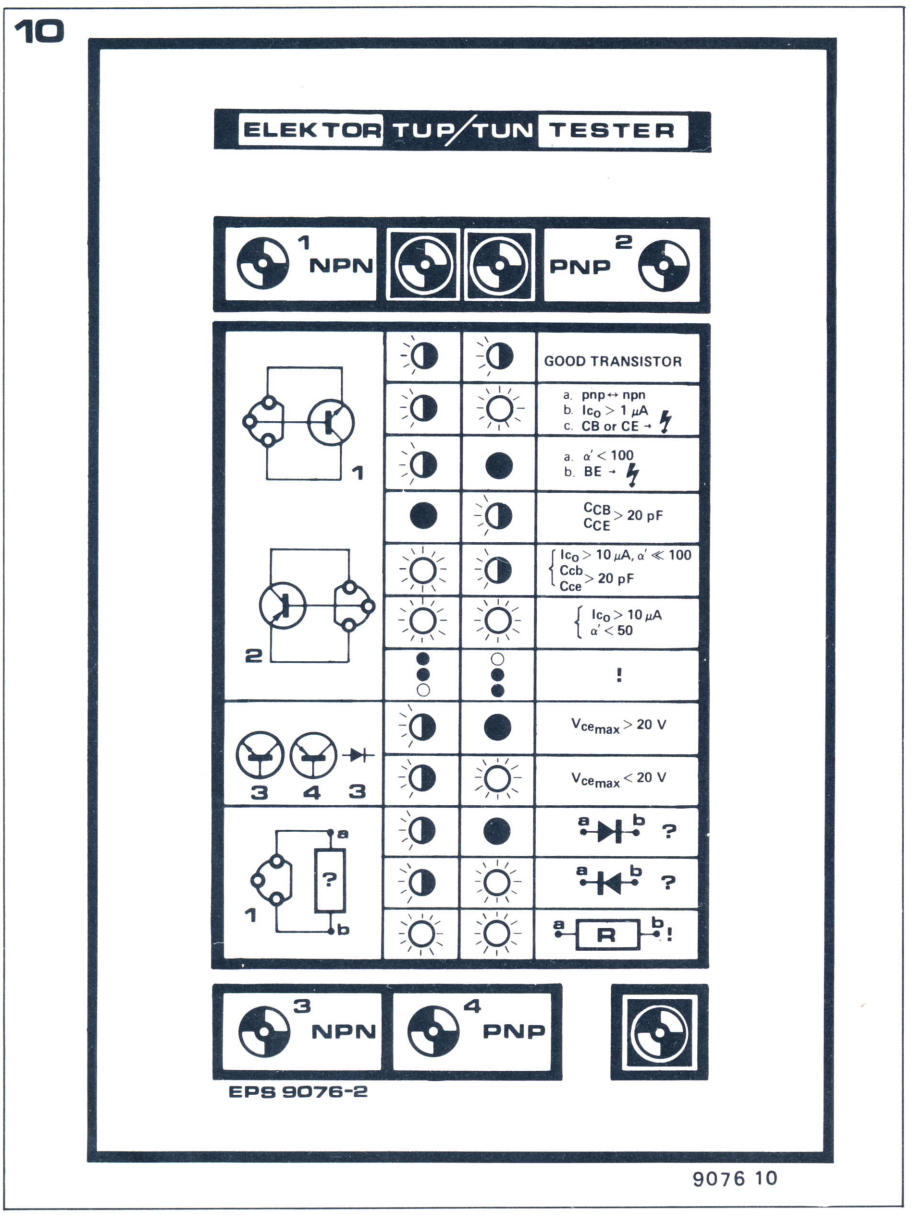


Figure 10. Front panel design for the tester. This panel is available via the Elektor print service, with black lettering on an aluminium-coloured background, as a self-adhesive label.

in the correct way round, i.e. that one has mistakenly connected it this way instead of reversing the connections. So it is important to make tests in both polarities if ambiguities are to be avoided.

If a diode which leaks moderately is plugged in the wrong way round, the leakage current may be enough to hold the anode of D10 positive while T10 is turned off, but not while T10 is turned on. This will give a display in which both LEDs appear to be on continuously – the same as for a transistor which is both leaky and low in current gain.

General

Figure 3 summarises the LED indications when the fast oscillator is on or off, and for different potentials at the anode of D10 in the main PNP testing section. The difference between this figure and table 1 is that the table is based on the fast oscillator and point 'A', which is common to the main testing circuits and to the breakdown voltage testing circuit. The relationship between the potential at the anode of D10 and the potential at 'A' when the main PNP testing section is in use is that a high potential at the anode of D10 produces a low potential at 'A' and vice versa. Figures 4, 5 and 6 summarise the meanings of the possible LED indications for various tests. Figure 4 is, of course, derived from figure 3. The front panel design (figure 10) summarises all three figures.

Construction and testing

Unless one has access to an independent means of testing the transistors and diodes, these should be ones which carry the manufacturers' warranty. Resistors should have 5% tolerance.

Figure 9 shows the p.c. board and the component layout for the complete tester (with the exception of the mains transformer). It should be noted that the emitter and collector connections to the test sockets appear to be interchanged, but when the sockets are mounted on the copper side of the board the connections will be correct. This facilitates the mounting of the board flush under the top panel, without the other components getting in the way. As it is not possible to give meaningful voltage or current test values for individual transistors, which might help to localise mistakes or faults, the construction should be checked very carefully. Even if one does not intend to use the optional LED 'C', one of the LEDs which will ultimately serve as 'A' or 'B' can be 'borrowed' at the constructional stage to serve temporarily as 'C' and thus give a check whether the slow oscillator (T2 and T3) and also T4 is working. The actual value of the nominally 680 Ω resistor in series with 'C' is not critical. If the temporary 'C' is seen to blink at about the right rate, test number 1 of figure 7 will show whether T8 is also working. Test number 2 will show whether T7, T9, T11 and T12 are working if the short is put into test socket T_A, and T7, T9, T13 and T14 with the short in test socket T_B.

To check the complete PNP and NPN testing sections, including the breakdown voltage test, one will need spare PNP and NPN transistors known to be sound, in addition to those used in building the tester. Only a transistor with normal current gain, or with a particular combination of faults, can produce a display in which LED 'B' blinks.

Once the two good transistors have been seen to give the display for test number 3 of figure 7, the more refined test number 4, which simulates the effect of excessive capacitance, can be applied. A 22 pF capacitor should be enough to make LED 'A' black out altogether, but it may be of interest to experiment with different lower capacitor values to find what value of capacitor is just low enough to allow the waveform at the junction of T_A and T10 to extend below the critical level (about 10 V) and cause LED 'A' to blink dimly, as shown in figure $3e_2$.

The emitter-base junction of a transistor forms a diode with a reverse breakdown voltage of about 5 V, so one of the transistors used in the foregoing checks can also be used to check the breakdown voltage testing section (figure 7; number 5). One must make sure that it is connected the right (or is it the wrong?) way round.

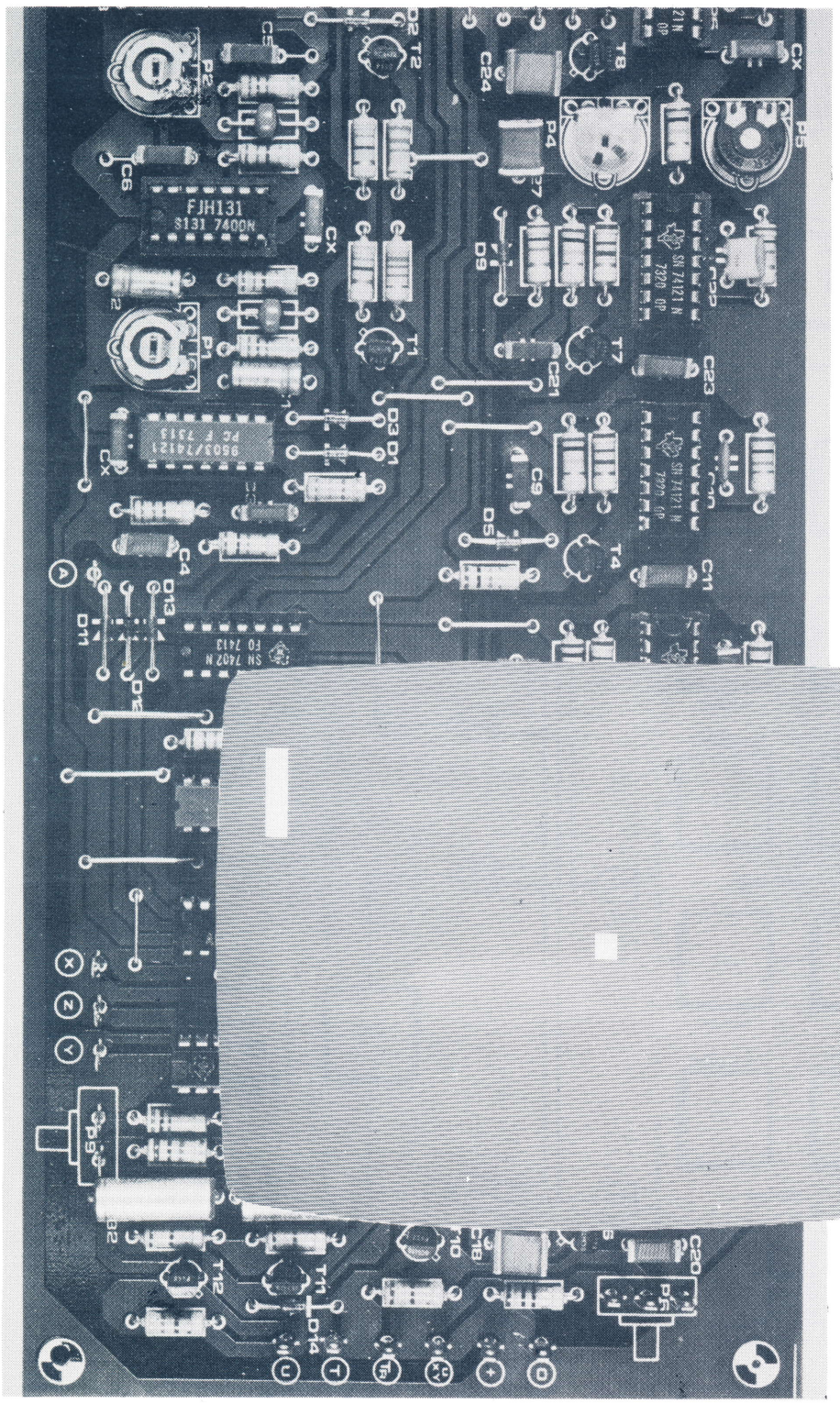
Power Supplies

Three different possibilities are offered for a mains power supply unit (figure 8): a simple unstabilised unit, a stabilised unit with the stabilisation circuit built up from three discrete components, or a stabilised unit using an IC. The unstabilised unit uses a transformer with an 18 V secondary – which may sometimes be difficult to obtain – and a 1000 μ capacitor. If either of the stabilisation circuits is used, the capacitor can be much smaller. The 20 V transformer used in these circuits should be more readily obtainable.

The transistor or IC should have a heatsink.

tv tennis

The popularity of television tennis games has prompted Elektor to produce a design that can easily be built by the home constructor for a modest cost. Although several designs have previously appeared on the market, it was felt that there was a need for a simple circuit using a minimum of components.



In order to keep costs down the TV tennis circuit generates the most basic 'picture' possible, i.e. two 'bats' and a 'ball'. The ball is 'served' from one side of the screen or the other and the players move their bats up and down the screen to intercept the path of the ball. If the ball strikes a bat it is returned, otherwise it leaves the side of the screen and a 'new ball' must be served. Should the ball reach the upper or lower edge of the screen during its traverse across the screen it will 'rebound'. The upper and lower boundaries are, however, not displayed on the screen.

The output of the TV tennis game is used to modulate a VHF oscillator so that the game may be plugged direct into the aerial socket of a television.

Principle of operation

For those not familiar with TV a brief resumé of the principles involved may prove helpful. A TV picture is, of course, generated by an electron beam scanning across the phosphor-coated face of a cathode-ray tube in a zig-zag fashion from top to bottom. At the end of each horizontal line the beam flies back to the left hand edge of the screen and starts the next line slightly lower down the screen. Each complete scan (frame) of the picture consists of either 405 or 625 lines, depending on the transmission standard. To reduce the bandwidth required to transmit the video information a complete frame is not transmitted in a single scanning of the picture, but is made up of two 'fields' containing half the number of lines in a frame. These two fields are interlaced with each other to make up a complete frame. Fields are transmitted at a 50 Hz rate, therefore frames are transmitted at half that rate, i.e. 25 frames per second.

The video waveform

In order to build up a picture on the screen the brightness of the trace must be modulated by varying the electron

beam current. This is controlled by the amplitude of the video waveform. So that the scanning of the electron beam in the TV set is in synchronism with the received signal in order to build up the picture correctly, field sync. pulses are transmitted (at the end of each field) and line sync. pulses are transmitted (at the end of each line).

To distinguish sync. pulses from video information, sync. pulses are negative-going and confined to a voltage below that required for zero beam current (black level). Video information occupies a range of voltages above black level up to the voltage required to saturate the TV tube phosphor (peak white level). Circuitry in the TV distinguishes between sync. pulses and video information. Field sync. pulses also have a longer duration to distinguish them from line sync. pulses.

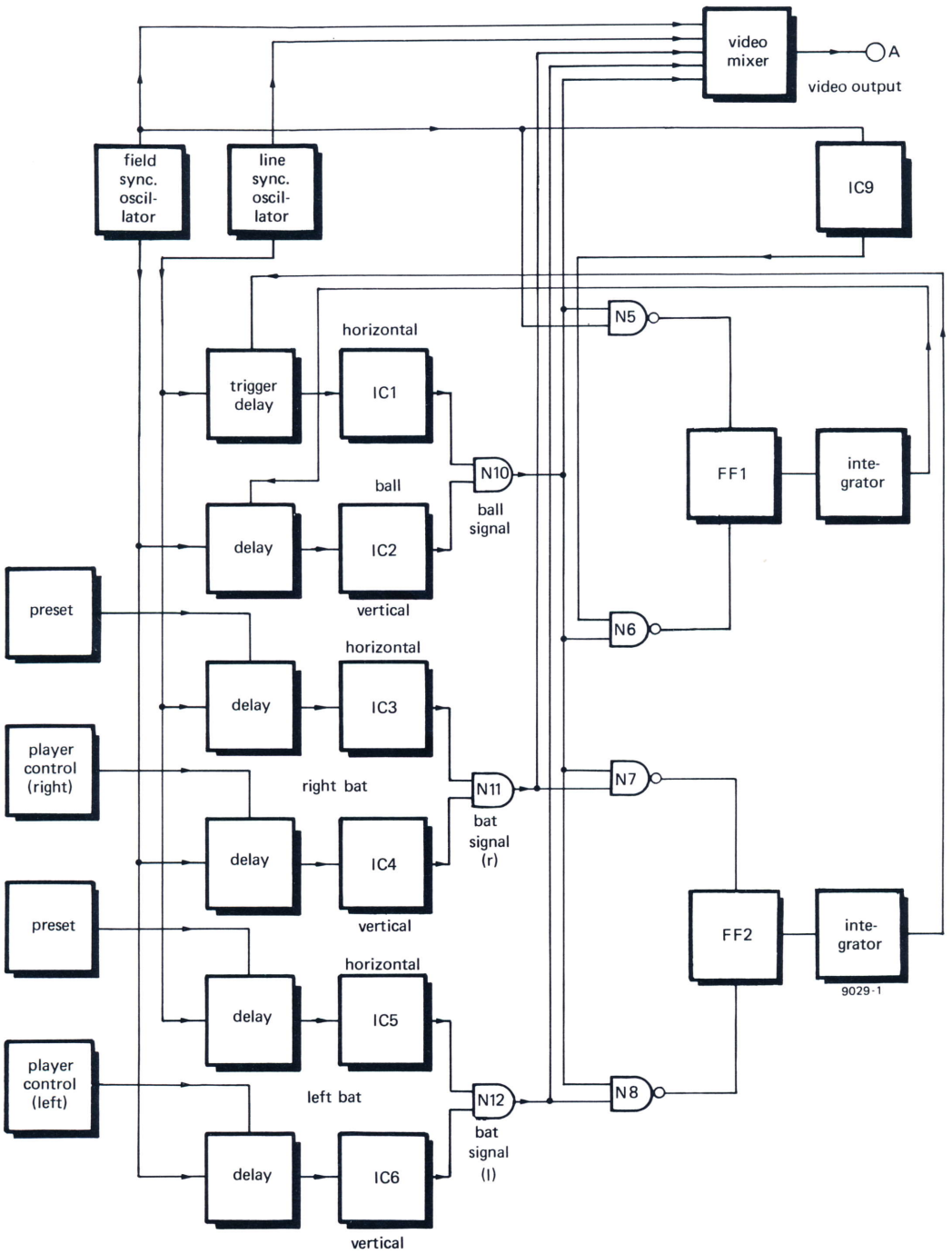
From the foregoing some of the requirements for the circuit become apparent. Firstly, the circuit must contain oscillators capable of generating field and sync. pulses at the appropriate frequencies (50 Hz and 15625 Hz respectively). Secondly, circuitry for generating the bat and ball waveforms, and for controlling the movement of these, is required. Fortunately, since we are concerned only with white bats and ball on a black background the only modulation required is peak white level or black level, so analogue circuitry is not needed to produce these waveforms, and digital logic circuits can be used to generate the rectangular pulses necessary.

Block Diagram

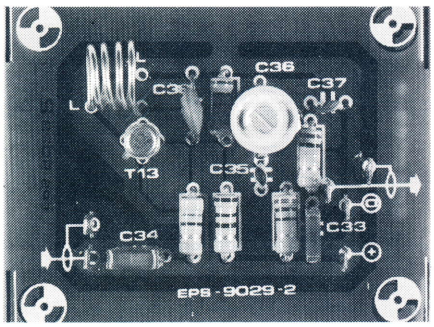
The operation of the circuit is best understood with the aid of a block diagram (figure 1). Sync. pulses from the field and line oscillators are mixed in the video mixer and then fed to the modulator. They are also used to control the timing of the other waveforms.

All the video waveforms are generated using monostable multivibrators and as the generation of the 'bats' is simplest this will be considered first. The left-hand player's horizontal bat generator IC5 is triggered continuously from the line sync oscillator. A presettable trigger delay is incorporated so that the pulse appears a little time after the line sync pulse. This ensures that the bat appears some way in from the left hand edge of

1



the screen. The right-hand player's horizontal generator IC3 incorporates a longer delay so that this bat appears near the right-hand edge of the screen. Since the triggering occurs after every line sync pulse the result would be a vertical band of white the full height of the screen. This is where the vertical bat generator (IC6 left, IC4 right) comes in. This monostable is triggered from the field sync pulses via a delay which is continuously variable by the player. This determines the vertical position of the bat. The delayed pulse from the vertical bat generator gates the pulses from the horizontal oscillator so that they are only allowed through for the duration of this pulse. The result is thus a vertical bar on the screen whose vertical position can be varied by the player and



whose height (length of the bat) is determined by the duration of the vertical pulse. The same applies for both the left- and right-hand bats.

The ball is generated in a similar manner with two monostables (IC1 and IC2). However, since the ball is continuously moving this in effect means that for movement to the right the horizontal trigger delay is increasing all the time, and for movement to the left it is decreasing.

For downwards movement the vertical trigger delay is increasing, while for upwards movement it is decreasing. Of course it is necessary to reverse the direction of ball travel when the ball strikes a bat or the upper and lower boundaries. This part of the circuit operates as follows:

the horizontal ball pulse generator (IC1) is triggered via a delay by the line sync pulses. The delay, and therefore the horizontal position of the ball on the screen, is controlled by the output of an integrator, which is fed with a d.c. voltage and therefore generates a ramp which varies the trigger delay linearly. The slope of the ramp (positive- or negative-going) and hence the direction of ball travel is determined by the state of flip-flop FF2. If FF2 is initially reset the ball will travel to the right. However, should the 'ball' output and the right-hand 'bat' output both be high at the same time (i.e. the ball strikes the right hand bat) then the output of N7 goes low, resetting FF2 and reversing the horizontal direction. When the ball strikes the left-hand bat then the output of N8 goes low, resetting the flip-flop and causing the ball

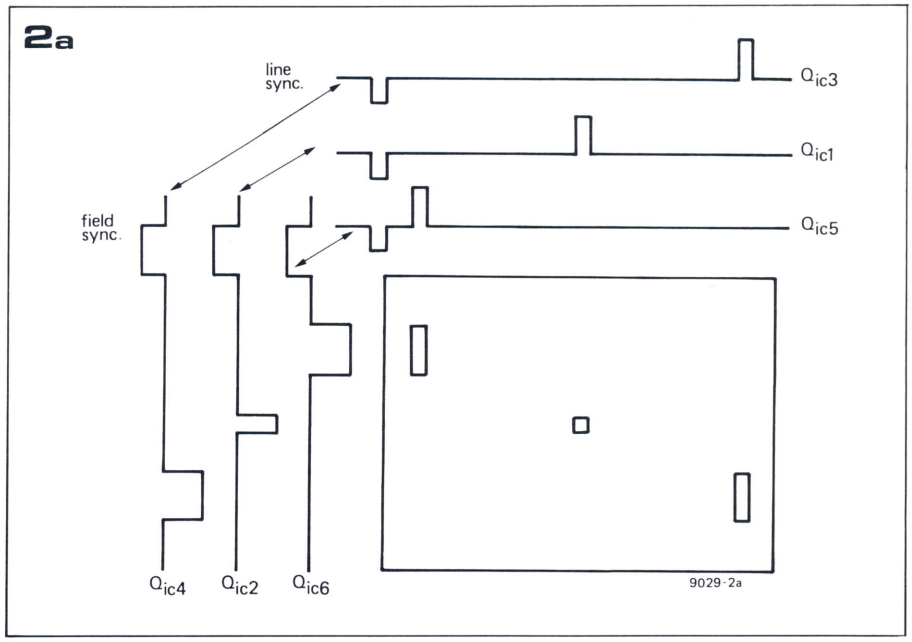


Figure 1. Block diagram of TV Tennis game (excluding modulator/oscillator).

Figure 2a. The horizontal and vertical waveforms are gated together as shown to produce the bat and ball display.

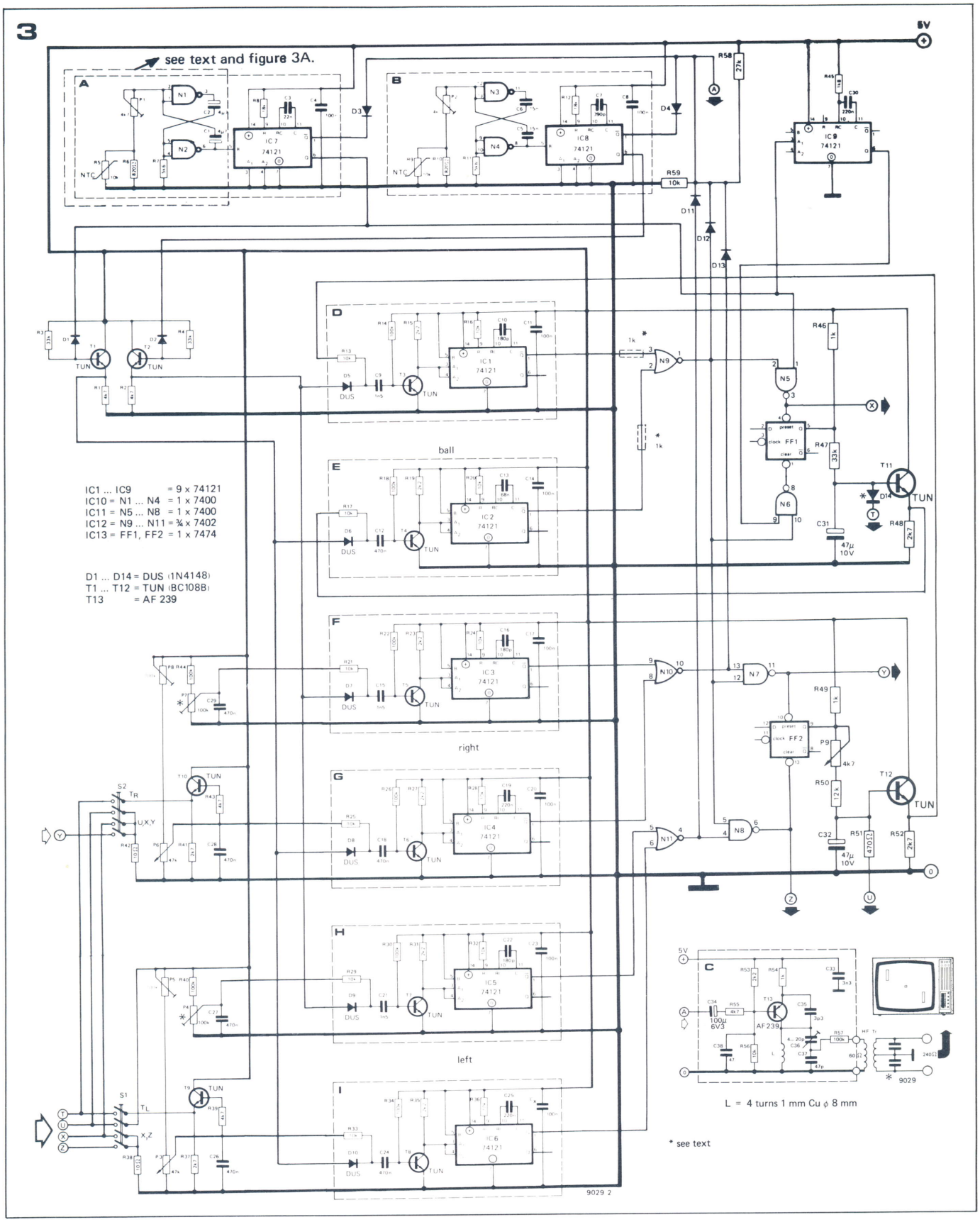
Figure 2b. The complete video waveform as seen on an oscilloscope.

to travel to the right. If the ball does not strike a bat it will leave the side of the screen and will not return until it is 'served', since the state of the flip-flop is not changed and the integrator output will eventually saturate in one direction or another. Service will be dealt with in the description of the full circuit.

Travel of the ball in the vertical direction is controlled in a similar fashion, but here the change of direction occurs at the upper and lower boundaries. The lower border of the picture corresponds with the leading (negative-going) edge of the field sync pulse, so change of direction at this boundary is accomplished by gating the ball signal with the field sync pulse in N5. To change ball direction at the top of the picture a monostable (IC9) is triggered by the trailing edge of the field sync pulse. The output pulse of the monostable is gated with the 'ball' signal to reset FF1. A timing diagram showing how the various pulses are gated together to produce the bat and ball outputs is given in figure 2, together with the general appearance of the complete waveform as seen on an oscilloscope.

Complete Circuit

The complete circuit is given in figure 3. Field sync pulses are produced by the circuitry in box A, which consists of an astable multivibrator driving a monostable to produce pulses of the correct length. Box B contains similar circuitry, but operating at a much higher frequency, to produce line sync pulses. The $\overline{Q}$ outputs of these monostables (to produce the negative-going sync pulses) are fed via D3 and D4


3
see text and figure 3A.
5V
A
B
C
D
E
F
G
H
I
IC1 ... IC9 = 9 x 74121
IC10 = N1 ... N4 = 1 x 7400
IC11 = N5 ... N8 = 1 x 7400
IC12 = N9 ... N11 = ¾ x 7402
IC13 = FF1, FF2 = 1 x 7474
D1 ... D14 = DUS (1N4148)
T1 ... T12 = TUN (BC108B)
T13 = AF 239
ball
right
left
L = 4 turns 1 mm Cu ϕ 8 mm
* see text
9029 2
9029

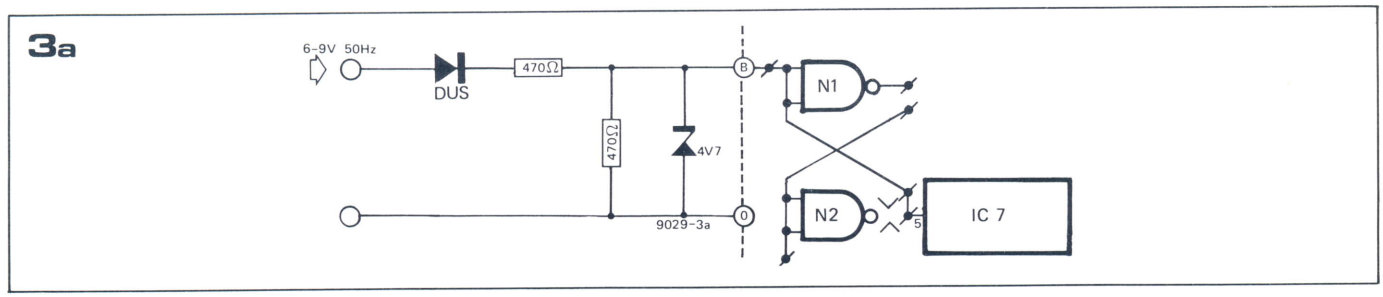
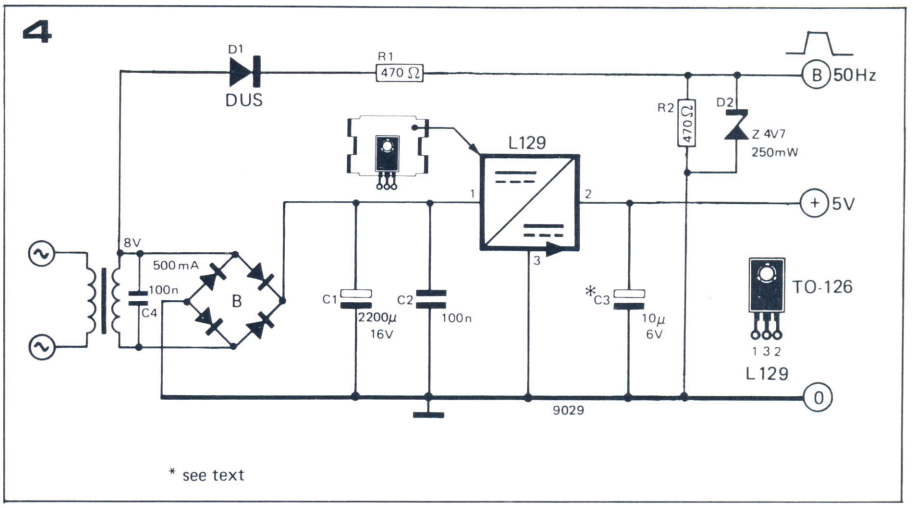

3a
6-9V 50Hz
DUS
470Ω
4V7
N1
N2
IC 7
9029-3a

Figure 3. The complete circuit of the TV tennis game. The modulator/oscillator circuit is shown inset at the bottom right-hand corner.

Figure 3a. Suggested modification to derive field sync pulses from the mains for mains only versions of the game. This should give a more stable picture than the free-running field oscillator, so it is highly recommended wherever possible.

Figure 4. Circuit of the mains power supply for TV Tennis.



Parts list for figures 3, 5 and 7

Resistors:
R1,R2,R39,R43,R55 = 4k7
R3,R4,R47 = 33 k
R5*,R9 = 10 k NTC
R6*,R10 = 820 Ω
R7,R11 = 5k6
R8,R12 = 18 k
R13,R16,R17,R20,R21,R24,R25, R28,R29,R32,R33,R36,R56, R59 = 10 k
R14,R18,R22,R26,R30,R34,R40, R44,R57 = 100 k
R15,R19,R23,R27,R31,R35,R53 = 2k2
R37,R41,R48,R52 = 2k7
R38,R42 = 10 Ω
R45 = 1k8
R46,R49,R54 = 1 k
R50 = 12 k
R51 = 470 Ω
R58 = 27 k
P1*,P2 = 4k7 lin. preset
P3,P6 = 47 k lin.
P4,P5,P7,P8 = 100 k lin. preset

Capacitors:
C1*,C2* = 4µ7, 10 V
C3 = 22 n
C4,C8,C11,C14,C17,C20,C23,C_X = 100 n
C5,C6 = 15 n
C7 = 390 p
C9,C15,C21 = 1n5
C10,C16,C22 = 180 p
C12,C18,C24,C26,C27,C28,C29 = 470 n
C13 = 68 n
C19,C25,C30 = 220 n
C31,C32 = 47 µ, 10 V
C33 = 3n3
C34 = 10 µ/6.3 V
C35 = 3p3
C36 = 4 . . . 20 p trimmer
C37,C38 = 47 p

Semiconductors:
T1 . . . T12 = BC547B, BC107, 2N3904
T13 = AF239
D1 . . . D14 = 1N4148
IC1 . . . IC9 = 74121
IC10,IC11 = 7400
IC12 = 7402
IC13 = 7474

Sundries:
L = 4 wdg. 1 mm ϕ Cu, ϕ 8 mm
HF Tr = 60 Ω → 240 Ω impedance converter (see text)

* see text

to the junction of R58 and R59. This portion of the circuitry fuctions as the video mixer. Black level occurs when the $\bar{Q}$ outputs of IC7 and IC8 are both high and the bat and ball inputs to D11, D12 and D13 are all low. The voltage at the junction of R58 and R59 is then solely determined by the value of these resistors and is about 1.35 V. When a sync pulse occurs then the junction of these two resistors is held down to about 1 V via D3 or D4. When bat or ball signals occur the inputs to D11, D12 or D13 go high, so the potential at the junction of R58 and R59 becomes about 4 V.

If the unit is to be used for mains only operation the astable in box A can be dispensed with and field sync pulses may be derived from the 50 Hz mains by the modification shown in figure 3a. P1, R5, R6, C1 and C2 are omitted; the sync pulses are fed in at the original connection to the positive side of C1 on the board, and the track between this point and the output of N2 (pin 6 of IC10) must be broken.

The sync pulses are buffered by emitter followers T1 and T2 to avoid loading the monostables excessively. The buffered sync pulses are then fed via the trigger delays to the appropriate monostables which generate the horizontal and vertical components of the bat and ball waveforms. The trigger delay circuits are all identical in principle and merely vary in component values. The trigger delay for IC3 operates as follows: normally T5 is turned on by base current through R23. Its collector voltage (and hence the A inputs of IC3) is low. The cathode of D7 is held at a few volts positive by the voltage via R21 from P7 (max. 2.5 V), and since T2 is turned off the anode of D7 is at 0 V. C15 thus has a voltage across it equal to the voltage on the cathode of D7 minus the base-emitter voltage of T5. On the leading edge of the line sync pulse T2 turns on, forward biassing D7. C15 thus charges until the voltage across it is

$5\ V - V_{beT2} - V_{D7} - V_{beT5} = 3\ V$

approximately. On the trailing edge of the sync pulse T2 turns off. The voltage on the cathode of D7 therefore reverts to its initial value (the potential supplied via R21 from P7). However, since the voltage across C15 is still 3 V then the base of T5 must be negative. T5 therefore turns off. C15 now charges via R22 until the voltage on the base of T5 reaches about 0.7 V when T5 turns on and the collector voltage goes low, triggering the monostable.

It is evident that the trigger delay is dependent on the time taken to charge C15 after T5 has been turned off, which is in turn dependent upon the voltage applied to the cathode of D7 from P7. The trigger delay may thus be varied by a d.c. voltage, in the case of the bats derived from the various potentiometers, and in the case of the ball from the emitters of T11 and T12.

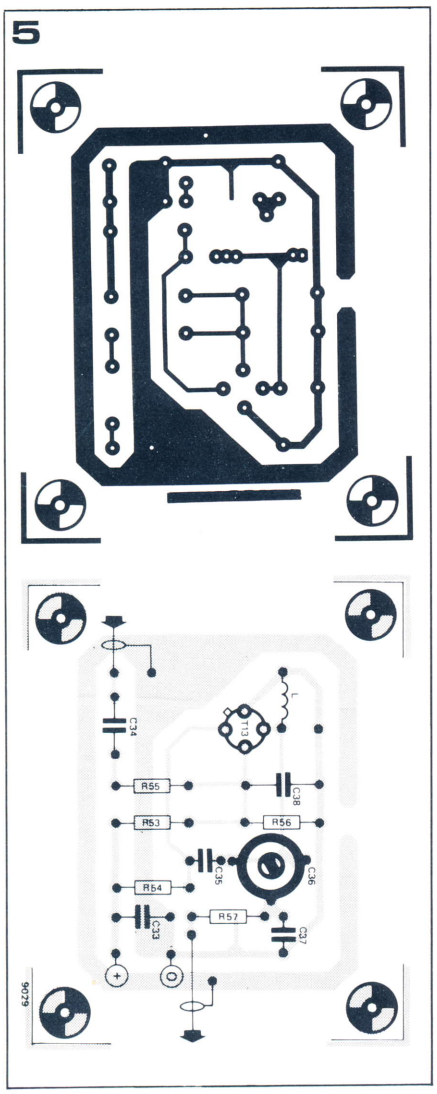
In the case of the ball, as explained earlier, the trigger delay in both horizontal and vertical directions is continuously varied to achieve motion of the ball. Horizontal movement of the ball is controlled by FF2 and the integrator constructed around T12. When FF2 is preset the Q output is high and C32 charges via P9 and R50. The potential on the emitter of T12 therefore rises. This is applied to R13, thus continuously increasing the trigger delay and making the ball move to the right. When FF2 is cleared (reset) then C32 discharges via P9 and R50. The voltage on the emitter of T12 falls, thus decreasing the trigger delay and making the ball move to the left. The rate of charge or discharge of C32, hence the speed of the ball, is determined by the setting of P9. Vertical ball movement is controlled in a similar manner by FF1 and T11. Note that in this circuit the AND-gates shown in the block diagram have been replaced by NOR-gates connected to the $\bar{Q}$ outputs of the monostables. This is of course exactly equivalent to AND-gates connected to the Q outputs (De Morgan's theorem).

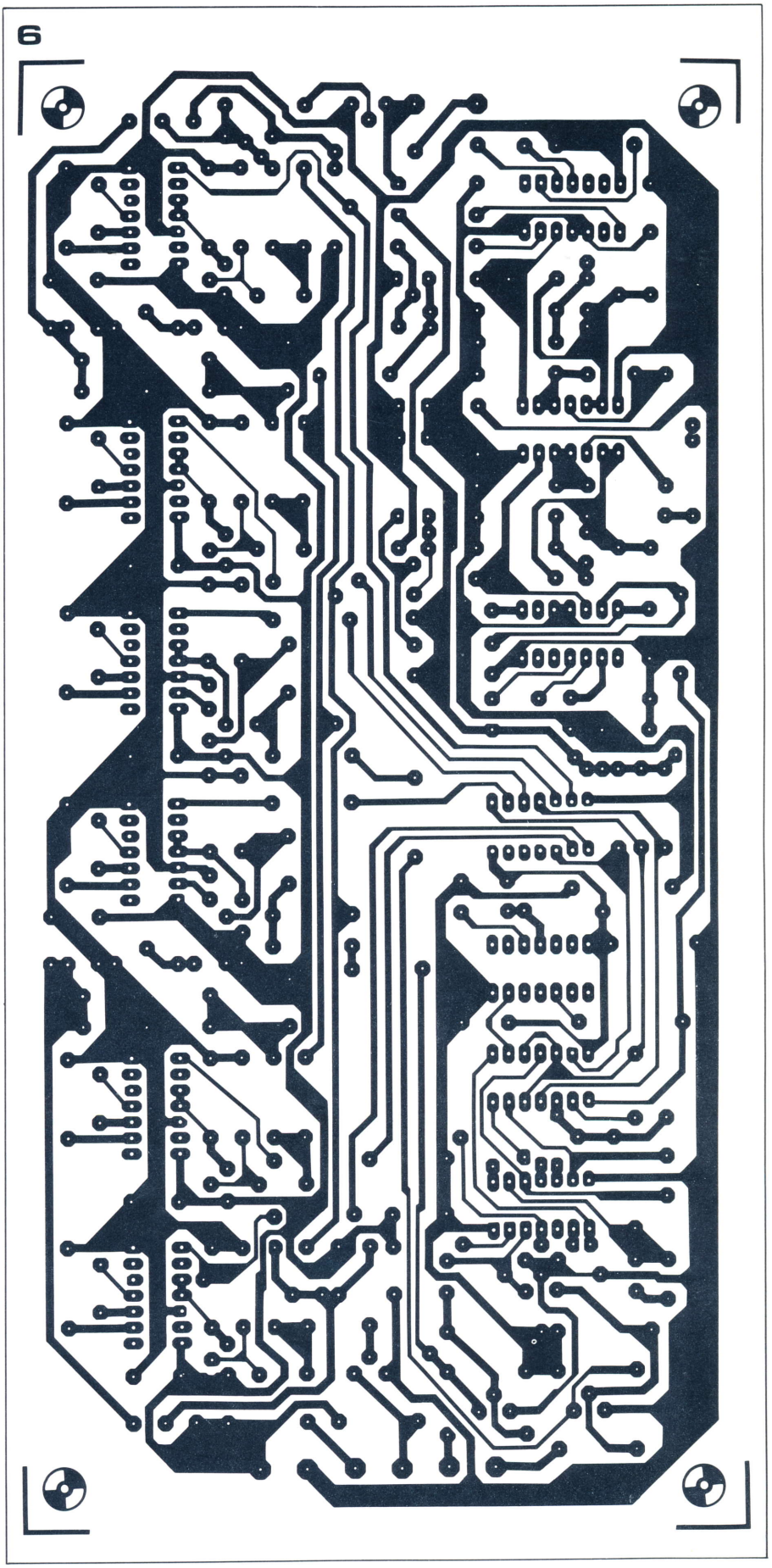
The horizontal bat trigger delays are preset,by P7 for the right-hand player, and by P4 for the left-hand player. This allows the position of the bats to be adjusted to a few cm away from the sides of the screen. The vertical position of the bats is continuously adjustable, by P6 for the right-hand player and P3 for the left-hand player. P5 and P8 are presets used to adjust the bat position

Figure 5. Printed circuit board and component layout for the modulator/oscillator circuit.

Figure 6. Printed circuit for the TV Tennis game.

Figure 7. Component layout for the main board. Note that the indications T3 and T4 are transposed!





so that P6 and P3 are effective over the full height of the screen.

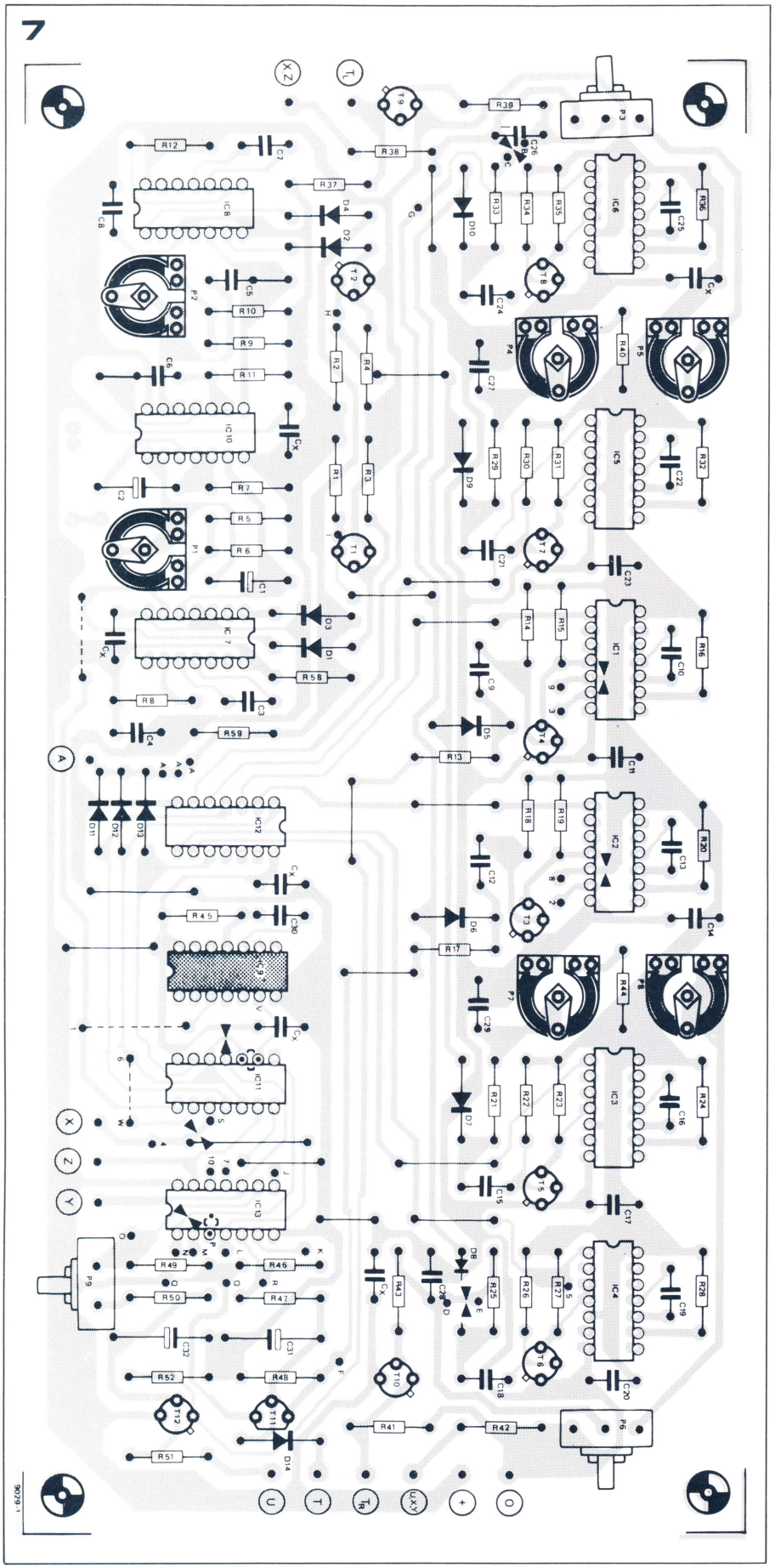
Service of the ball

It is evident that if the state of FF2 is not reversed by a coincidence between the ball and one of the bat signals then the voltage at the emitter of T12 will continue to rise or fall as C32 either charges or discharges, until it reaches either zero volts or supply minus the base-emitter voltage of T12. The ball will then disappear off one side of the screen or the other and will not return. For this reason (as well as for the rules of the game) it is necessary to 'serve' the ball when this has occurred.

Ideally the ball should emanate from the bat of the player who is serving. However, in practice this is difficult to achieve as it means that at the instant of service the vertical ball trigger delay must be matched to the vertical bat trigger delay. Since the delay circuits are independent component tolerances will make this unlikely. It is, however, possible to make the ball service dependent upon the bat position at the time of service, though not coincident with it.

Service is accomplished as follows:

for a service by the left-hand player the 4-pole switch S1 is closed. This produces several results. Firstly points X and Z are connected to ground via R38. This clears FF1 and presets FF2 so that when the ball is served it will travel upwards and to the right.



7

Point U (R51) is connected to positive supply, thus charging C32 rapidly and holding the ball off the left-hand side of the screen. Point T (cathode of D14) is connected to the emitter of T9, whose base is fed via R39 from P3 (left-hand bat control). The voltage on C31 is thus constrained to slightly above the emitter voltage of T9, thus determining the vertical position from which the ball will start. When the switch is released the constraints on C31 and C32 are released so the ball travels in a direction determined by the states of FF1 and FF2 (i.e. up and to the right).

Service by the right-hand player operates, so to speak the same way but backwards, i.e. pushing S2 grounds point X so that the ball still travels upwards. However, point Y is grounded so that the ball travels to the left, and point U is grounded to discharge C32 so that it starts from the right. The vertical starting position is determined by the emitter potential of T10.

Modulator and oscillator

The only part of the circuit which remains to be described is the modulator/oscillator which converts the video output at point A into a VHF signal suitable for feeding direct into a television aerial socket. This part of the circuit is shown inset in figure 3. An AF239 forms the basis of the oscillator circuit which is tuned to the required frequency by the coil L and C36/C37. The output may be fed direct into an unbalanced 50 - 75 Ω coaxial cable terminating in a normal TV coax plug, or if the TV has continental type 240 - 300 Ω twin feeder input then the output must be fed through an inverse balun transformer before feeding into the 300 Ω feeder.

Power Supply

A power supply which is absolutely free from mains ripple is absolutely essential for the TV Tennis game. The reason for this is fairly obvious. Any mains ripple will cause a variation in the input voltages to the trigger delay circuits, and hence in the trigger delays. This produces distortion of the picture as the trigger delay varies down the screen height.

The 5 V power supply shown in figure 4 is strongly recommended. It uses an L129. However an LM309 can be used and is recommended when the additional TV tennis circuits are going to be added. This power supply is short-circuit protected. If another supply is to be used it must also be short-circuit proof, since when both 'serve' bottons are pressed simultaneously R42 and R38 are connected across the supply – the current consumption then becomes more than 1 A.

It has been found that some fixed voltage stabilisers actually supply approximately 4.8 volts. The consequence may be that practically the entire field remains white. The circuit of figure 4A shows how this can be remedied by raising the voltage.

4a

To minimise power dissipation within the IC it is recommended that a transformer with a 6.3 V RMS secondary voltage be used. This will give a DC input to the IC of about 9 V. The bridge rectifier is made up of 4 1-amp diodes such as 1N4001. Note that C3 should be a tantalum type to reduce output noise and any tendency to R.F. instability. Components D1, D2, R1 and R2 correspond with figure 3a.

Construction and adjustment

The p.c. board and component layout for the VHF oscillator are given in figure 5, for the main board in figures 6 and 7, and for the power supply in figure 8. Note that there are several indications on the main board that concern future extensions. At this stage these can be disregarded; the wire links shown dotted are all needed for the basic game.

Slider potentiometers are used for the bat controls as these give easier control than rotary types and are sufficiently robust for domestic use. The oscillator is mounted on a separate board as it must be housed in a completely screened box to avoid radiated interference and to minimise pickup of other transmissions. A small diecast or pressed aluminium box with a lid is suitable. The main board housing should also be a metal box. Having checked that the circuit is correct and that the power supply is giving the correct voltage before connecting it to the unit, power can then be applied and the output of the VHF oscillator plugged into a TV set. Due to the harmonics generated extending into the hundreds of MHz the unit will function on both VHF and UHF although we do not advise using the circuit on 405 lines VHF, as this calls for extensive modifications to the line sync and horizontal bat and ball position circuits.

Alignment, step 1:

Initially all the potentiometers should be set at the middle of their travel. If an oscilloscope is available the waveform at point A can be checked, if not, then proceed as follows. For UHF operation the TV set should be tuned to the low end of the UHF band. By adjusting the TV tuning and C36 it should be possible to tune in the signal. At first the picture will be rather chaotic as the field and line sync oscillators are not running at the correct frequency.

Alignment, step 2:

By adjusting P1 it should be possible to obtain vertical lock, i.e. the picture will stop 'rolling'. Of course with mains field sync there is no adjustment and if lock is not obtained it will be necessary to adjust the frame hold control on the TV set. It may be found that, due to the tolerances of C1 and C2 it is not possible to obtain the correct field sync frequency. The oscillator may run at 25 Hz, in which case the picture will

Parts list for figures 4 and 8

Resistors.
R1,R2 = 470 Ω

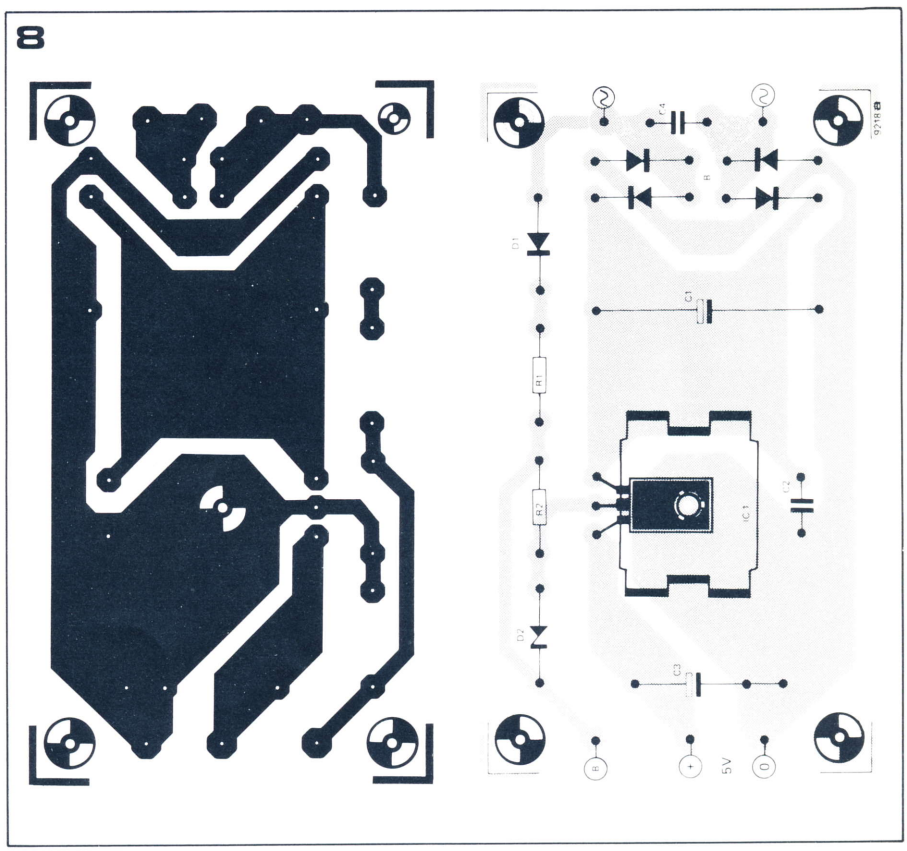
Capacitors:
C1 = 2200 μ/16 V
C2,C4 = 100 n
C3 = 10 μ/6 V (tantalum)

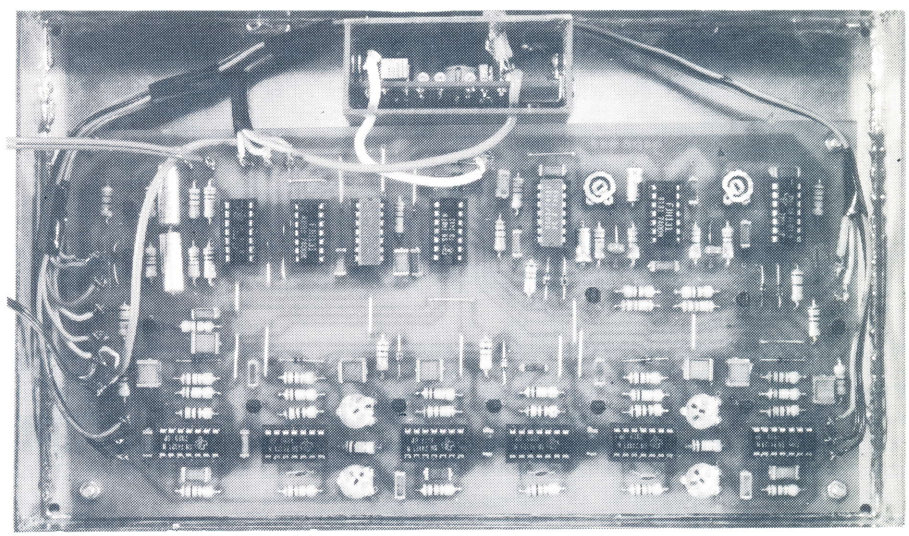
Semiconductors:
D1 = DUS
D2 = 4.7 V zener
B = Bridge rectifier, or 4 x 1N4001
IC1 = L129, LM309 (5 V/1 A)

Sundries:
Transformer, 6.3 V (r.m.s.) secondary

Figure 7A. Shows where to connect the line sync pulses from the power supply board.

Figure 8. Printed circuit board and component layout for the power supply.





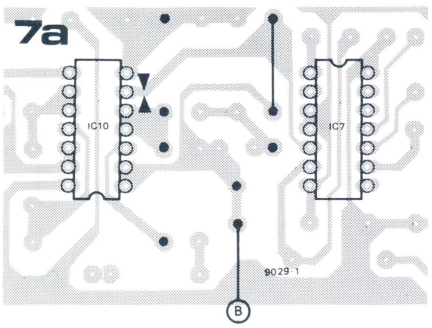
lock but will jitter considerably. In this case C1 and C2 should be reduced to 2µ2. It may be found that a black bar appears in the centre of the screen. This is because the field sync oscillator is running at 100 Hz, and P1 should be adjusted until normal lock is obtained. Having obtained vertical lock the picture will probably consist of a random pattern of white dashes.

Alignment, step 3.

P2 can now be adjusted until the two bats appear on the screen. If the line sync oscillator is tuned to a multiple of the line frequency then four bats may appear.

Alignment, step 4.

Having obtained the correct number of bats the horizontal positions of the left- and right-hand bats may be adjusted by P4 and P7 respectively.



Alignment, step 5:

The final adjustment is to the range of the vertical bat controls. With the slider controls set to the centre of their travel P5 and P8 are adjusted so that the bats are halfway down the screen. It should now be possible to traverse the bats over the entire screen height, and some further slight readjustment of P5 and P8 may be necessary to achieve this.

The unit is now ready for use and it should be possible to serve a ball from either side of the screen by pressing the appropriate service button. Due to the simple nature of the circuit it may be found that pressing the service button causes slight picture jitter, but this should not prove inconvenient in practice.

Trouble-shooting

Some readers have encountered problems involving vertical distortion of the picture. This can be caused by poorly adjusted horizontal synchronisation, so a word of advice will not be out of place: first of all re-read the adjustment instructions given.

Carefully check all wiring and other connections, then set all pre-set potentiometers to mid position and carry out the alignment procedure as described. If this does not cure the problem, some further 'brute force' expedients are required:

- the three ICs in the synchronisation circuits (IC7, IC8 and IC10) are sensitive to interference pulses on the positive supply rail. For this reason it is advisable to run completely separate wires from the supply electrolytic (in the power supply shown in figure 4, this is C3) to each of these ICs. The simplest way to do this is to unsolder the positive supply pins (pin 14, in each case), bend the pins up from the board and solder the wires on to them in mid-air. The positive supply ends of the decoupling capacitors (C8, C_X and C_X) are also unsoldered from the board and connected via 1 Ω resistors to pin 14 of the corresponding ICs.
- the negative supply to IC10 (pin 7) could also do with some additional decoupling. A 100 µH micro-choke in series with this connection is sufficient. The easiest way to mount this is to unsolder all seven pins on that side of the IC and bend it up so that these pins are in mid-air (pins 1 to 6 are no longer used after the mains sync has been incorporated). The choke is then mounted between the original hole for pin 7 and pin 7 itself.
- if the frame sync is derived from the mains as recommended, there is a wire link in the connection between pins 1 and 2 of IC10 and pin 5 of IC7 (figures 3A and 7A). If a 2.2 mH choke is used in place of this link, some further improvement of picture quality can result.
- in some cases, the ball signals interfere with the other signals – causing a dent in the vertical boundaries that moves up and down with the ball, for instance. To prevent this, two 1 kΩ resistors can be added in series with the inputs of N9 (pins 2 and 3 of IC12). On the board, these resistors can be mounted in place of the original wire links between pin 2 of IC12 and pin 1 of IC2 and between pin 3 of IC12 and pin 1 of IC1 respectively.
- sometimes a minor improvement of the picture can be obtained by adding small resistors (1 . . . 2.2 Ω) in series with the decoupling capacitors C4, C8, C11, C14, C17, C20, C23 and C_X. The improvement depends on how 'lossy' the capacitors were in the first place.

The next item to receive attention is the ball speed. With the existing circuit it is impossible to obtain exactly the same ball speed in both directions. This is not so important in the vertical direction, but different ball speeds in the horizontal direction give one player an unfair advantage. Adjustment to equalize ball speeds in the left-right, right-left, and up-down, down-up directions may be provided by a 4k7 preset in series with R46, and a similar one in series with R49.

One other thing:

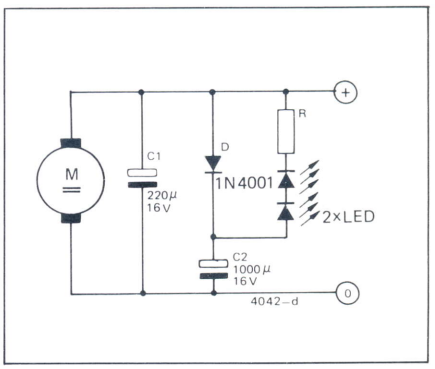
To cope with the additional load imposed by future extension circuits, the output capability of the emitter follower buffers T1 and T2 can be improved by changing the values of R1 and R2 to 1 k and R3 and R4 to 3k3.

R. Zimmer

brake lights for model cars

This circuit performs two functions: when the supply voltage to the motor of the model car cuts out, the car will not stop abruptly but will continue over some distance and during that time two LED's will light up and function as brake lights. Thus a very realistic effect is obtained. The circuit is extremely simple. As long as the car is under power, there is a voltage across the motor (M), the polarity of which is indicated in the diagram. Capacitor C_1 and (via diode D) also C_2 are now charged.

When the voltage cuts out, C_1 discharges



across M and C_2 discharges via the two LED's, resistor R, and motor M. If braking is the result of a short-circuit of the supply voltage, both capacitors discharge via the short-circuit connection; in that case the LED's burn somewhat brighter. The value of resistor R can be calculated with the following simple formula:

$$R = \frac{12 - 2.V_{LED}}{I_{LED}}$$

Usually a value of about 560 Ω will be suitable.

supplies for cars

In order to function effectively, electronic equipment used in cars must have an appropriate power supply, which in addition to providing a regulated voltage from the battery supply, must also suppress interference appearing on the battery voltage from the car electrical systems.

Two power supplies will be described; a simple zener stabilizer with built-in suppression, for low-power circuits such as instruments (electronic tachometer etc.) up to about 170 mA and a high-power stabilized supply, for powering such things as portable cassette recorders, up to about 2 A.

Low-power circuit

Figures 1 and 2 show the low-power circuit configuration for negative- and positive-earth cars respectively. L1 and D1 provide high-frequency decoupling. L1 may be wound on a wire-ended cylindrical ferrite core, with a diameter of about 10 mm, using 45 turns of 0.5 mm enamelled copper wire (25 SWG). Zener diode Z1 stabilizes the output voltage at 5.6 V, which is suitable for TTL circuitry, but 5.1 V or 4.7 V types would also do, as they are within the supply voltage limits for TTL. Other voltages may, of course, be used for different equipment.

If a supply voltage is required that is almost equal to the available battery voltage, then R1 and the zener diode may be omitted. Of course, the circuit will then not provide stabilization of the supply voltage, but only interference suppression. This would be quite adequate for COSMOS IC's, which are fairly tolerant of supply voltage variations.

The difference between battery voltage and output voltage is dropped across R1. In the example given, for a 6 V battery R1 would be 8.2 ohm ¼ W, and for a 12 V battery 47 ohm 2 W.

C2 should be a low-inductance type such as ceramic and D1 can be any diode that will carry 200 mA.

High-Power Circuit

This circuit (figure 3) is designed to provide a stable, interference-free supply for cassette recorders, audio amplifiers and other equipment. Car radios generally have their own inbuilt suppression circuits.

The circuit is a simple feedback stabilizer. T5 and T6 form a differential amplifier with a constant-current emitter load (T7). This compares a portion of the output voltage at the slider of P1 with a reference voltage provided by D6. T3 provides a constant current through this zener diode.T4 is a constant-current load for the collector of T6, which drives the Darlington-connected transistors T8 and T9. Current limiting is provided by T1 and T2. When the current through R4 is such that the voltage drop across it exceeds the base-emitter voltage of T1, this transistor turns on, which turns on T2, pulling down the collector of T6 and reducing the drive to T8. The maximum output current required determines the value of R4:

$$R_4 = \frac{0.5}{I_{max}} \ (\Omega)$$

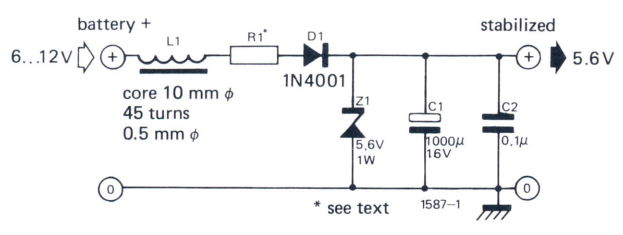
L1 is wound from 45 turns of 1.0 mm copper wire (19 SWG) on a ferrite core and thus provides interference suppression due to its high inductance. P1 will adjust the output between about 5.6 V and 12 V, although the higher figure can only be obtained when the (12 V) car battery is fully charged and in good condition, so that the supply voltage is around 14 V, since some voltage must be dropped across the series regulator transistor and R4.

A printed circuit layout for this supply is given in figure 4. The connections shown encircled in figure 3 are shown on the board layout. The circuit of figure 3 is for use with negative earth cars, but may be modified for positive earth simply by reversing all diodes and electrolytic capacitors and replacing transistors by their complementary equivalents.

If higher output currents are required, an external transistor (e.g. MJ3055) can be added. The connections to this transistor (T10) are shown dotted in figure 4; it should be mounted on an adequate heatsink, with mica washers for isolation. If this transistor is not required, the connections 5 and 6 on the pcb must be bridged.

To avoid deterioration of the board in the car due to humidity and dirt it is best to encapsulate the circuit (once it has been tested) in epoxy resin or silicone rubber.

1



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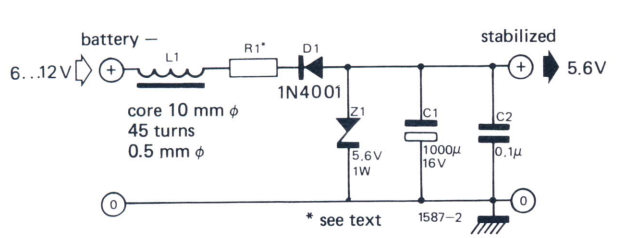

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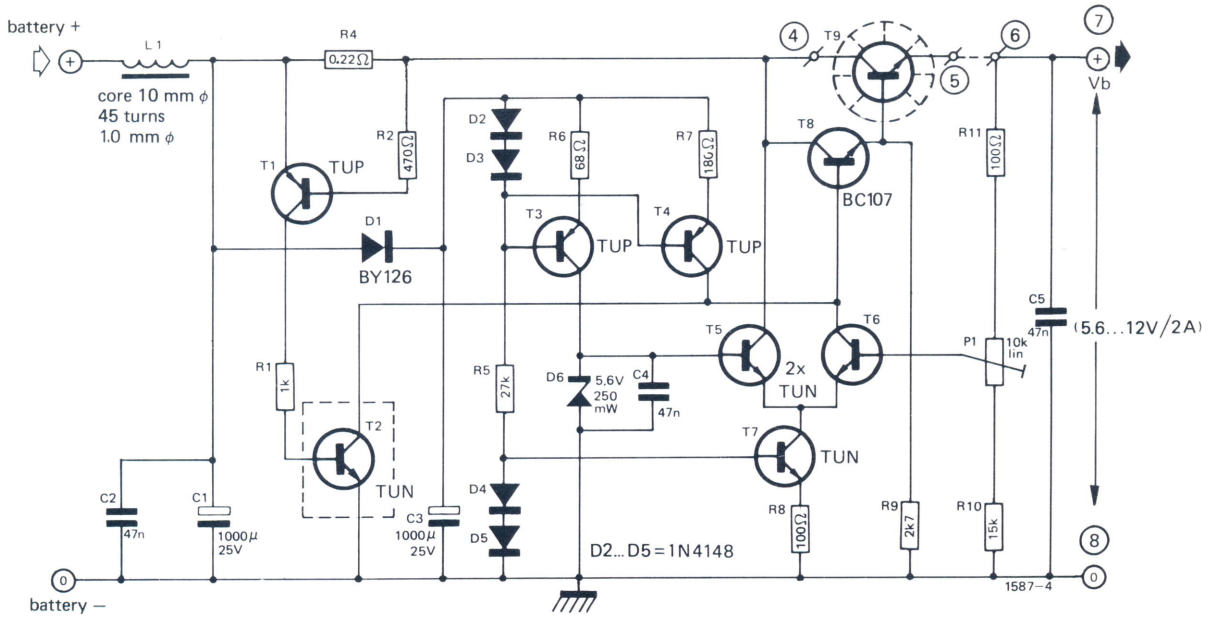


Parts list for figures 3 and 4:

Resistors:
R1 = 1 k
R2 = 470 Ω
R4 = 0.22 Ω*
R5 = 27 k
R6 = 68 Ω
R7 = 180 Ω
R8,R11 = 100 Ω
R9 = 2k7
R10 = 15 k
P1 = 10 k, preset

Capacitors:
C1,C3 = 1000 μ/25 V
C2,C4,C5 = 47 n

Semiconductors:
T1,T3,T4 = TUP
T2,T5,T6,T7 = TUN
T8 = BC107 or equ.
T9 = BD 131 or equ.
(T10 = MJ3055 or equ.*
D1 = BY 126
D2 ... D5 = 1N4148
D6 = 5.6 V/250 mW zener

Coil:
L1 = 45 turns of 1.0 mm enamelled copper wire on 10 mm ϕ ferrite former.

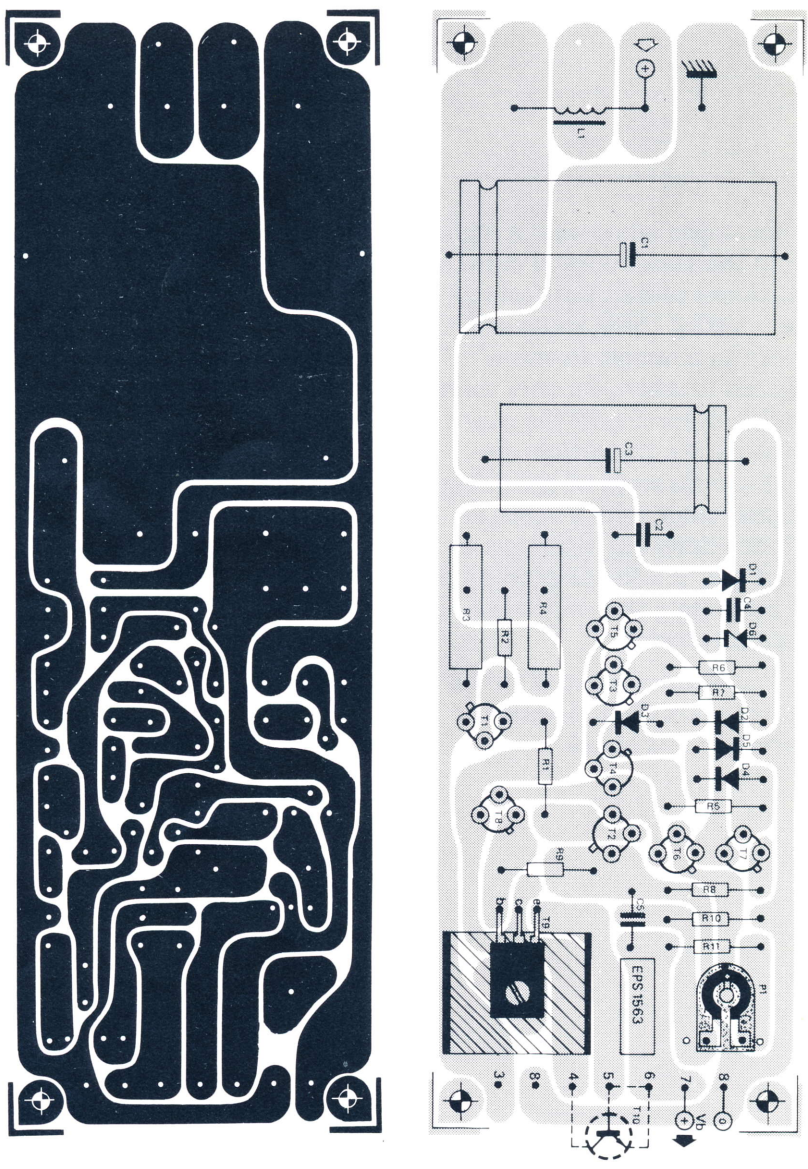
* see text

Figures 1 and 2. Simple zener stabilized supply with high-frequency suppression. Figure 1 is for negative earth and 2 is for positive earth.

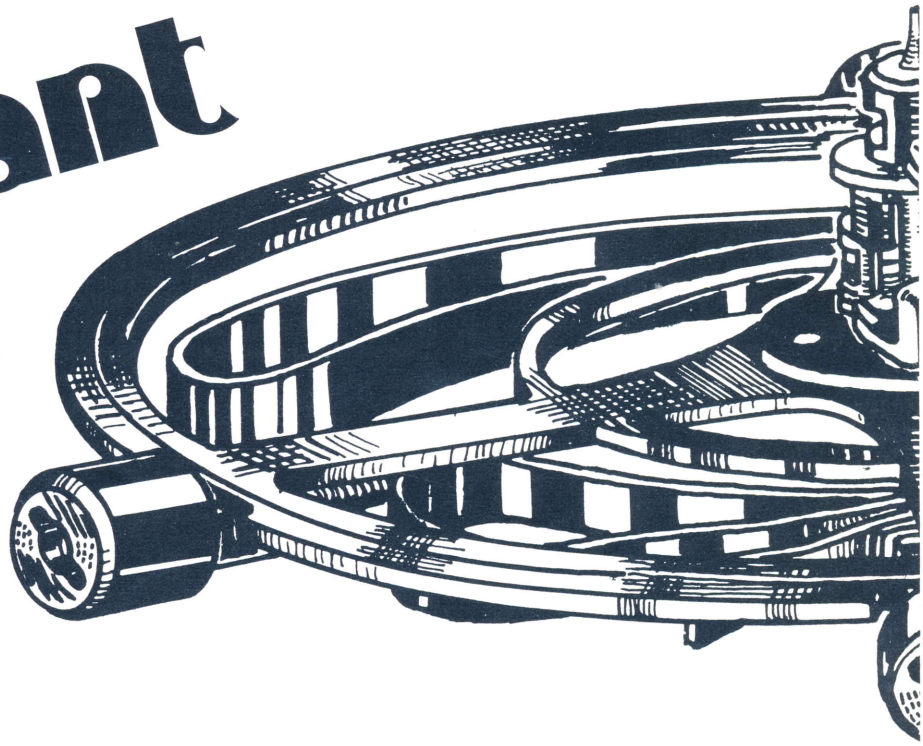
Figure 3. A high-power regulated supply for car electronics. The output voltage may be adjusted from 5.6 V to 12 V and the circuit will supply 2 A continuously.

Figure 4. P.c. board and component layout for the circuit of figure 3.

4



clamant clock



Any horologist who keeps a digital clock in the same room as conventional clocks cannot but feel sad to see it sitting there, mute and reproachful amongst its more vociferous brothers, its only sound the feeble humming of the mains transformer. In this article we look at various ways of providing the digital clock with a voice, so that it can draw our attention to the fact that it is keeping time far more accurately than any mere mechanical clock.

(These units can be added to the versatile digital clock described elsewhere in this book)

The main attribute lacking in a digital clock is the comforting tick which assures us that the thing is actually going. How many man-hours have been wasted waiting for the elusive change of that last digit? 'Well I'm sure its been stuck at that time for more than a minute now.'

A clock with a seconds display or flashing colon alleviates these problems, but the hypnotic effect of such devices has been known to send people to sleep. No such problem exists with a tick, which informs us that the clock is working without actually looking at it.

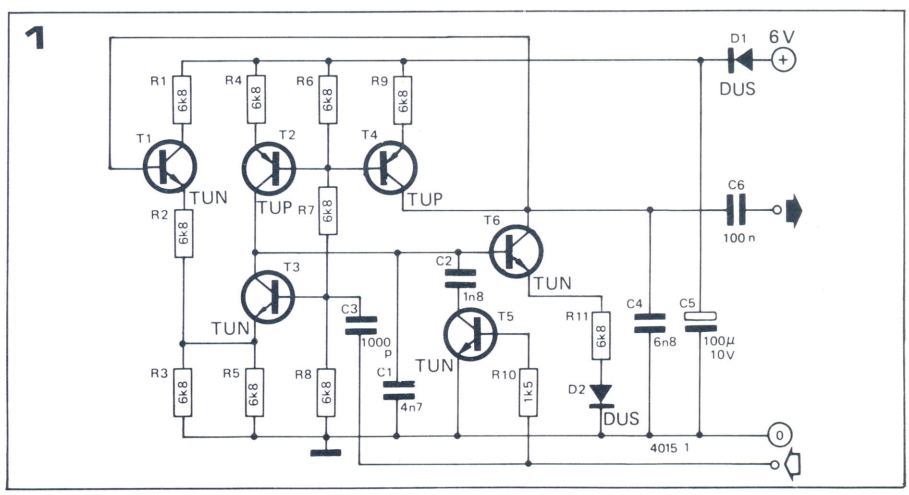
The tick-tock circuit

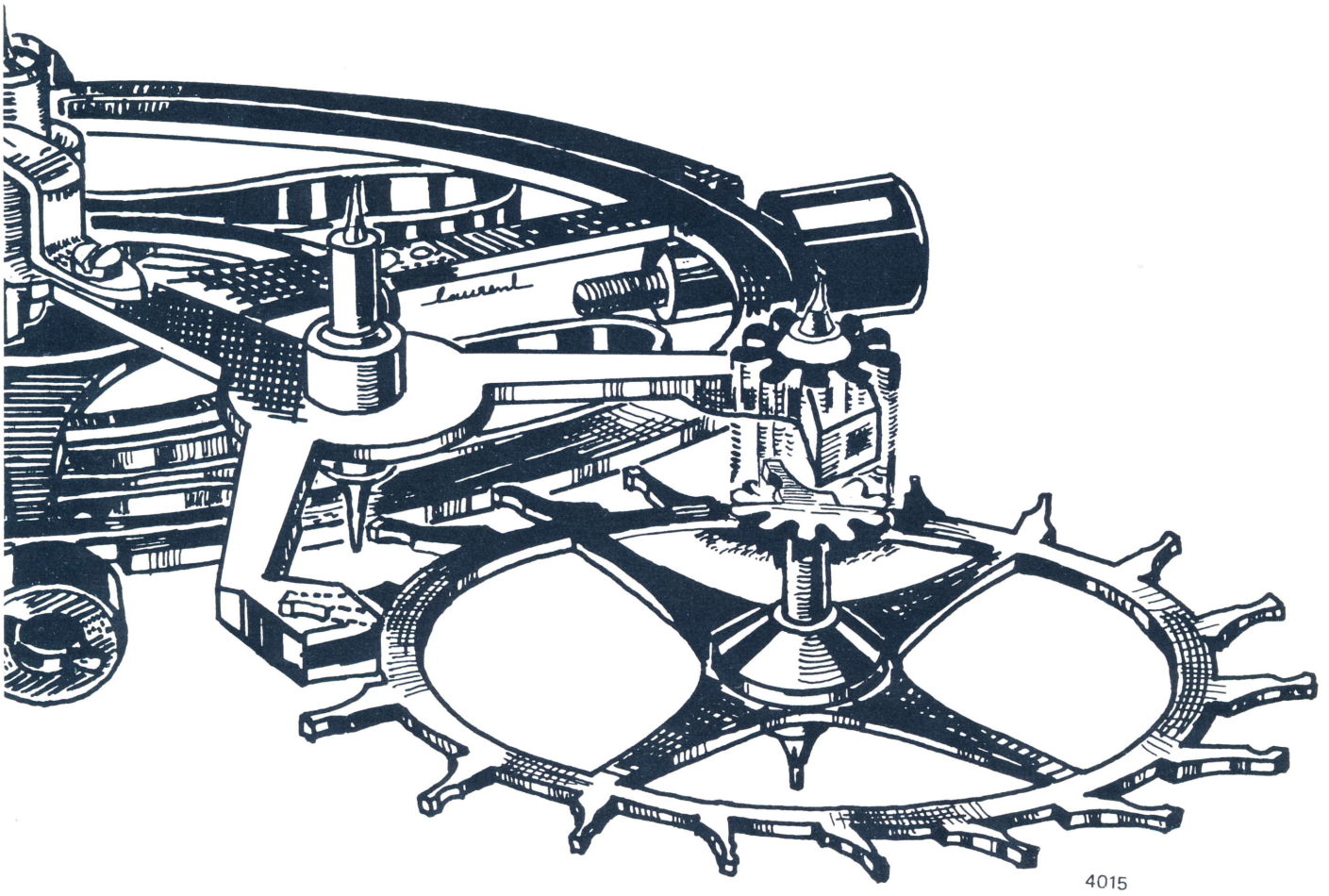
The tick-tock sound of a conventional clock is produced by the balance wheel (or pendulum) and escapement, the tick and tock sounds having different pitch. The pitch of the sounds and the repetition frequency obviously depend on the physical construction of the clock. A grandfather clock will have a deeper, more leisurely tick than a travelling alarm.

Electronic simulation of the sound is fortunately relatively simple. The waveform of the ticking is a damped res-

Figure 1. Gyrator circuit to simulate tick-tock of a clock.

Figure 2. P.C. board and component layout for gyrator circuit.





onance similar to a percussion instrument. A suitable circuit is therefore the gyrator used in the Elektor Minidrum (february 1975). This circuit (with the component values modified for this application) is given in figure 1. Suitable 1 Hz trigger pulses may be obtained from the clock circuit by taking an output from the counter preceding the seconds counter (either side of S3 in the versatile digital clock). The pulses must be TTL compatible (5 V amplitude) and have a 1 : 1 mark-space ratio, otherwise the ticking will sound unbalanced. The pulses are fed into the base of T3 through C3 to trigger the gyrator, whilst T5 switches C2 in and out of circuit to alter the relative frequency of the tick and tock.

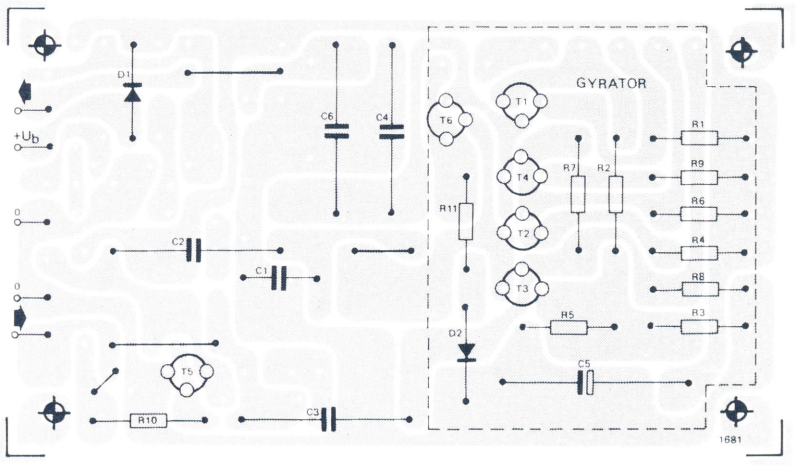
Components list for figure 1

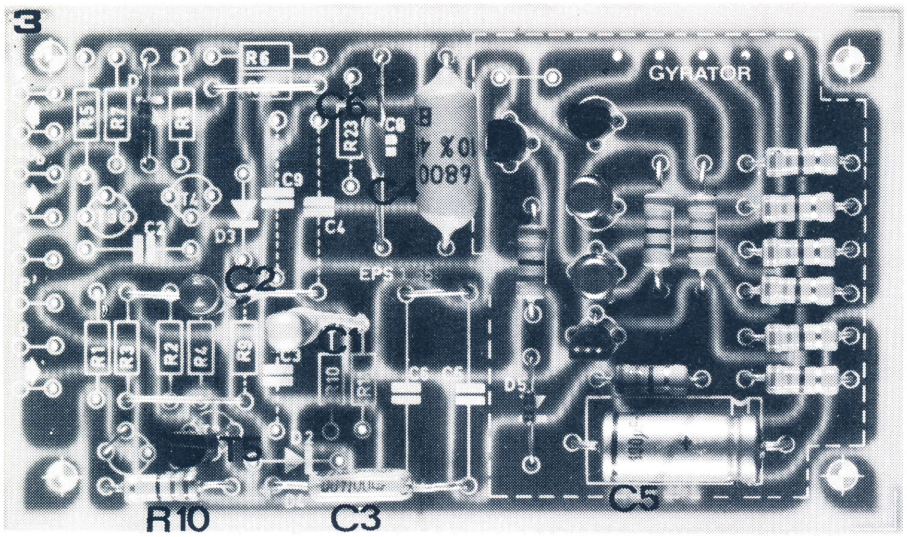
Resistors:
R1 ... R9,R11 = 6k8
R10 = 1k5

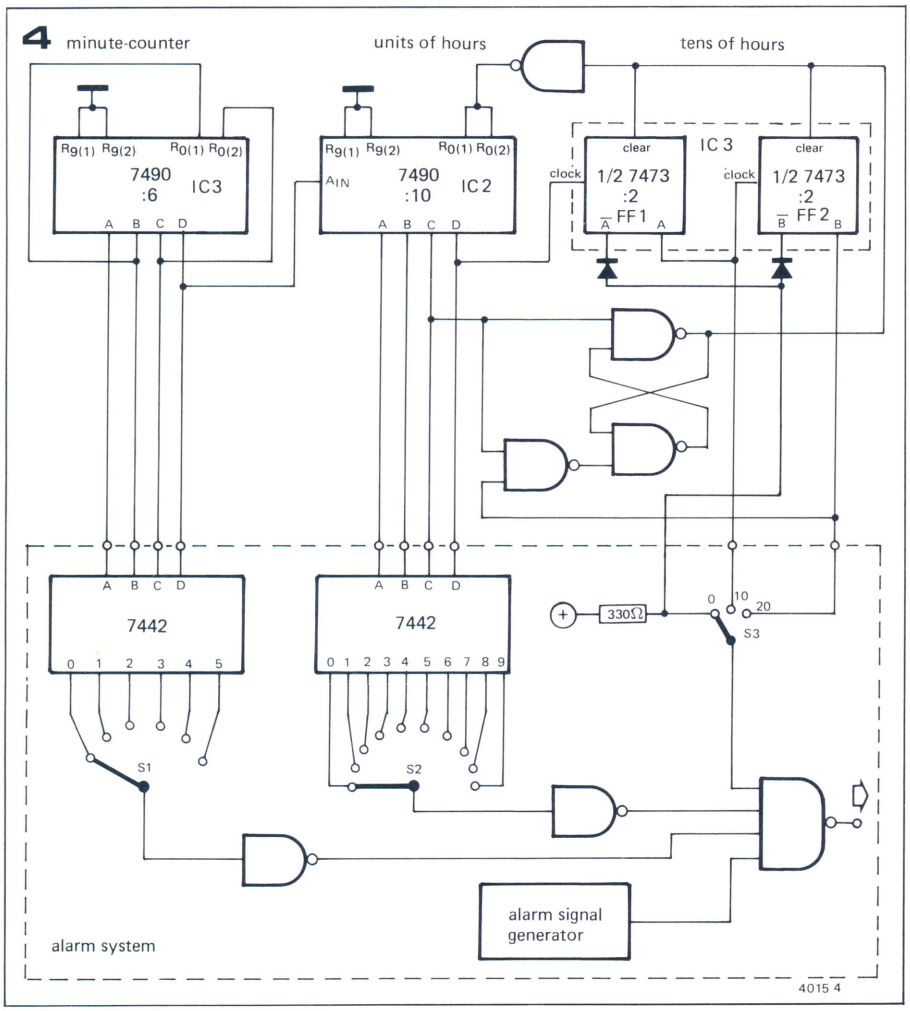
Capacitors:
C1 = 4n7
C2 = 1n8
C3 = 1 n
C4 = 6n8
C5 = 100 μ/10 V
C6 = 100 n

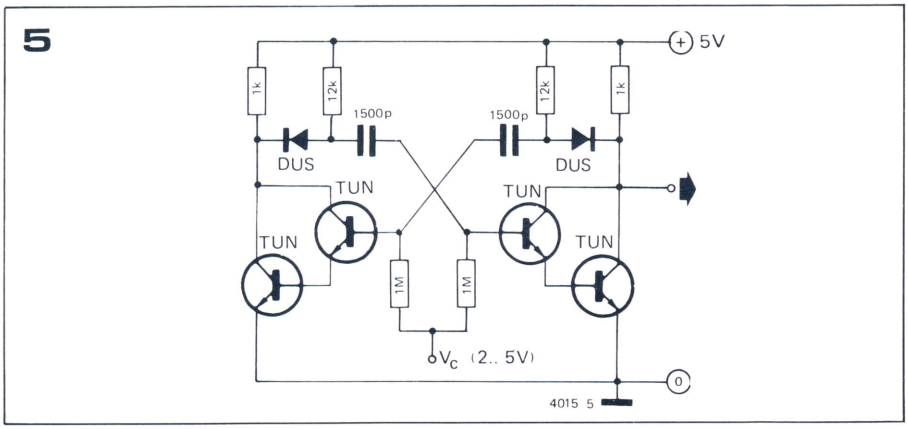
Semiconductors:
T1,T3,T5,T6 = TUN
T2,T4 = TUP
D1,D2 = DUS

2









The frequency of the sounds may be adjusted to suit personal taste by experimenting with the values of C1, C2 and C4. Since C3 and the input impedance of the trigger input differentiate the trigger pulse, changing the value of C3 will affect the 'crispness' of the sound.

P.C. Board

A suitable printed circuit board already exists for the Minidrum gyrator, and the board and component layout (modified for use with clock) are given in figure 2.

Alarm Clock

One clock noise in popular demand by readers (though perhaps not first thing in the morning) is an alarm. It is a simple matter to add an alarm to a digital clock (but unfortunately not so simple if the display is multiplexed). The alarm control circuit given in figure 4 is suitable for TTL clocks with parallel outputs (i.e. where the BCD outputs of the hours and minutes counters are available continuously and are not strobed). It was felt that an alarm setting accuracy of one minute was not necessary, so the smallest step provided in this circuit is 10 minutes.

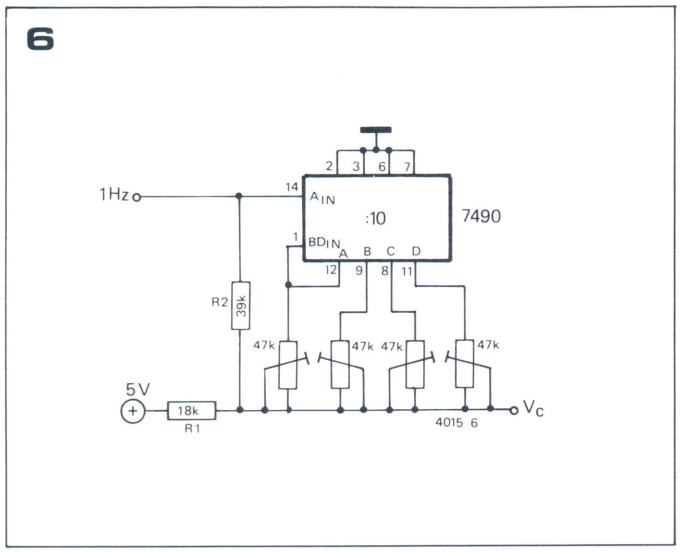
The circuit operates as follows:

the portion of the circuit inside the dotted box is the alarm. The rest is the existing clock circuitry. The BCD outputs of the hours and tens of minutes counters are decoded to decimal by the 7442's. No decoding of the tens of hours is required as the truth table for this counter (table 1) shows. Outputs A and B are never both '1' at the same time. The desired alarm time is selected by single-pole switches S1 - S3. When the required time is reached three of the inputs of the four-input NAND gate go high. This allows the alarm signal connected to the fourth input to pass through the gate.

The possibilities for the actual alarm signal generator are endless. The simplest solution would be a fixed frequency oscillator such as an astable multivibrator. There are however more interesting possibilities. The voltage-controlled multivibrator of figure 5 can be made to play a tune by connecting differing voltages sequentially to the control input. For a control voltage range of 2-5 V the frequency range covered is about 3 octaves. There are various methods of driving the oscillator. A simple circuit is shown in figure 6. This consists of a 7490 connected as a BCD decade counter, with its outputs connected to the VCO via presets. As the

Table I

HOURS	A	$\overline{A}$	B	$\overline{B}$
0	0	1	0	1
10	1	0	0	1
20	0	1	1	0



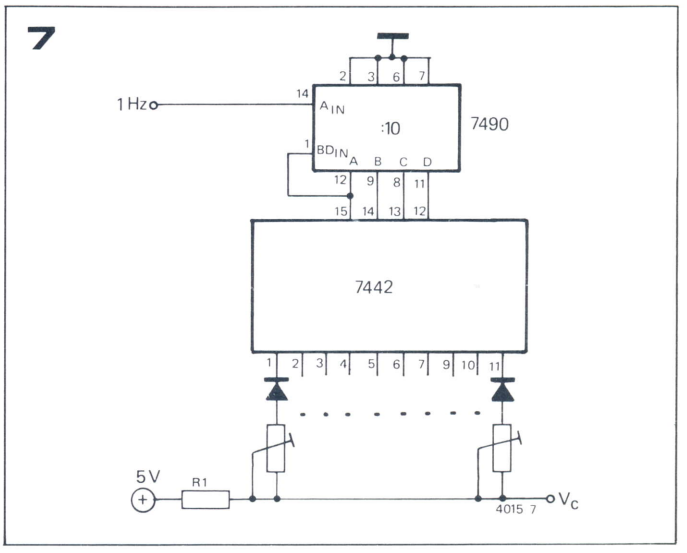


Figure 3. Photograph of the completed board that makes the tick-tock sound.

Figure 4. Circuit of an alarm control system.

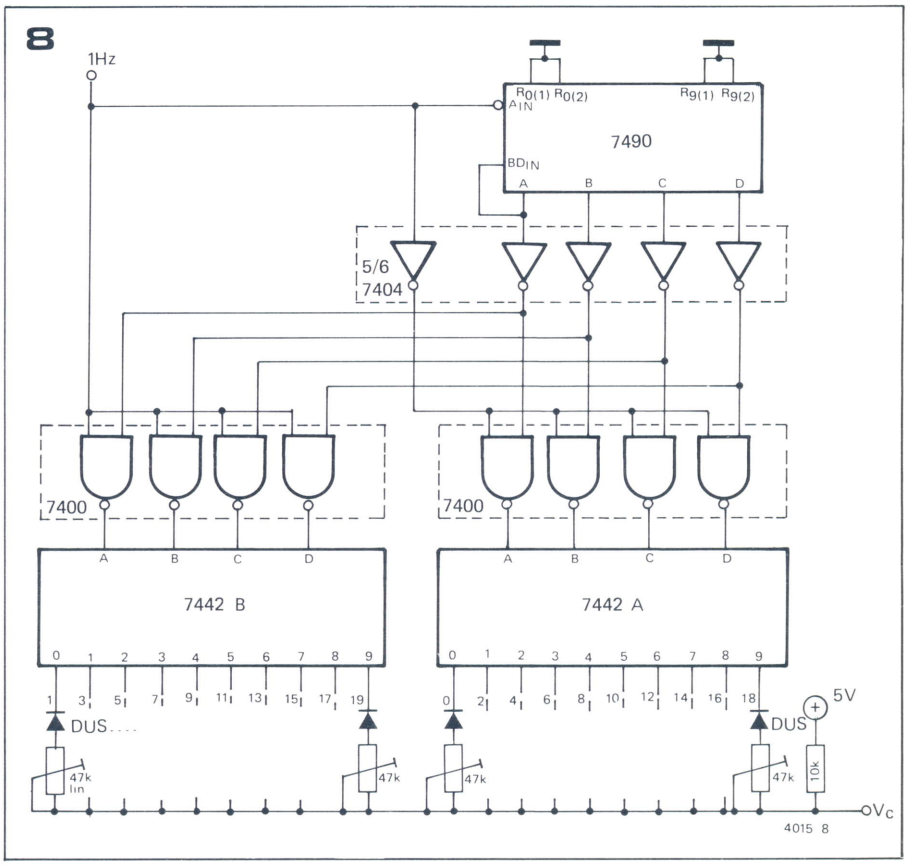
Figure 5. A voltage-controlled oscillator VCO that may be used to generate a tuneful alarm signal.

Figure 6. Using the existing seconds counter in the clock to produce a varying voltage for the VCO. Since the outputs interact it is difficult to tune this circuit to play a particular melody.

Figure 7. This circuit may be used to make the VCO play a tune. Ten independent sequential outputs are produced, so each preset can be used to tune one note in the sequence.

Figure 8. Extension of the circuit of figure 7 to a 20-note sequence.

Table I. Output of an arbitrary tens of hours counter as in figure 4.



output states of the counter change so will the output voltage to the VCO. Of course the outputs change in a binary sequence so more than one output can be high at one time.

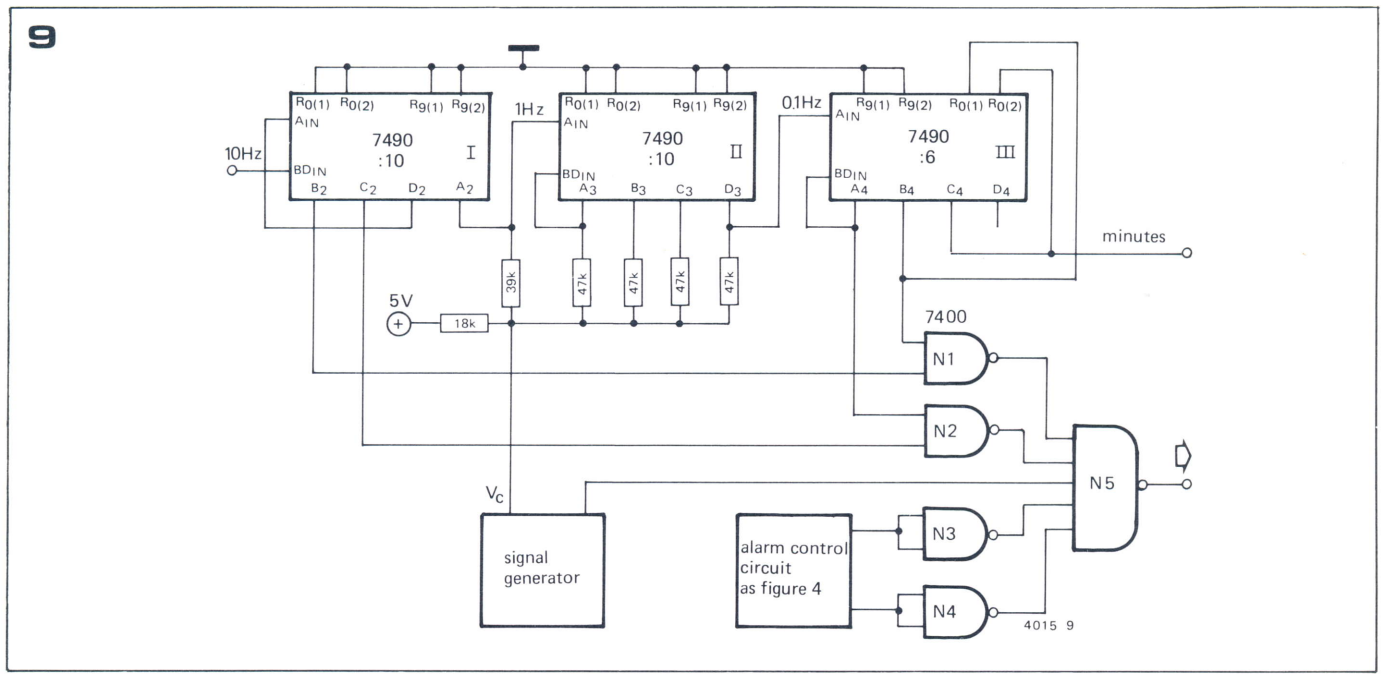
Since the outputs interact it is difficult to set this circuit to play a particular tune. In addition the 1 Hz clock pulses are also fed in via R2 increasing the permutations still further.

If one requires a circuit which can be set to play a particular tune then figure 7 is more suitable. Here the outputs of the 7490 are decoded with a 7442 to give ten independent outputs. These outputs go low in sequence as the counter goes through its cycle. All other outputs are high, reverse-biassing their respective diodes, so no current flows through their respective presets. Only the preset connected to the output which is low forms a potential divider with R1. This means that each note in the sequence can be tuned independently.

This ten-note sequence can easily be extended to twenty notes by the circuit of figure 8. In this circuit two decoders are driven by the 7490 and are switched in and out by the 1 Hz clock pulses to the counter. Thus, during the half-period when the clock pulse is '0' the outputs of the 7490 are switched through the transfer gates (7400) to decoder A. The other transfer gates are disabled by the '0' on their commoned inputs, so their outputs are all '1'. This is an invalid input code for the 7442 so all its outputs are high. During the '1' half period of the clock pulse the reverse situation occurs. Decoder B is enabled,whilst A is disabled. Decoder A thus controls the even notes 0, 2, 4, . . . in the sequence, whilst decoder B controls the odd notes 1, 3, 5, ... Of course in this case, if an equal time span is required for each note then the clock pulse waveform must have a 1 : 1 mark-space ratio. The 7490 in all these cases can be the existing seconds counter (IC6) in the clock.

Another variation on the alarm theme can be obtained by a circuit which changes the rhythm of the tone sequence, making it less monotonous. Such a circuit is given in figure 9. The dividers I to III are again part of the existing clock circuit (IC9, IC6 and IC5). The operation of the circuit is as follows:

counter II controls the pitch of the voltage controlled multivibrator as in the circuit of figure 6, except that no adjustment is provided for. The time at which the alarm sounds is again determined by the alarm control circuit, as in figure 4. The rhythm variation is



provided by gating the C output of counter I with the A output of counter III, and the B output of counter I with the B output of counter III. This has the following effects. Starting at a point in the timing cycle where counter III has just reset, A_4 and B_4 are both '0'. The outputs of N1 and N2 are thus high so (assuming it is time for the alarm to go off and the outputs of N3 and N4 are high) the tone sequence controlled by counter III can pass through N5. After 10 seconds output A_4 goes high and the pulses from output C_2 switch the output of N2 between '0' and '1'. The tone from the output of N5 is thus switched on and off at a 2.5 Hz rate. After 20 seconds output B_4 goes to '1' whilst output A_4 goes to '0'. The output of N2 is thus high whilst via N1 output B_2 switches the tone on and off at a 5 Hz rate. After 30 seconds output A_4 again goes to '1' while B_4 remains at '1'. Outputs B_2 and C_2 therefore both affect the tone output. When either of these outputs is high the tone is off, and when both of them are low the tone is on.

A timing diagram for these events is shown in figure 10. The top two waveforms are the outputs B_2 and C_2 during a 1 second interval of the sequence (this repeats every second). The other 4 waveforms are the tone outputs that occur for the four possible states of A_4 and B_4.

The audible effect is thus as follows:
an uninterrupted tone sequence for 10 seconds, then a further 10 second interval of tone bursts and silence as in figure 10d, then 10 seconds as figure 10e and finally 10 seconds as in figure 10f, after which the sequence repeats. Of course, during each ten second period the frequency of the tone is being varied by the outputs of counter II.

It should be noted that for all these alarm circuits a symmetrical 1 Hz squarewave is required from the output of counter I. This means that the 7490 (which consists of a divide-by-2 and a divide-by-five counter in the same package) must be connected with the divide-by-2 after the divide-by-5, as shown in figure 9. If an existing clock circuit is used this counter may be connected as a BCD decade counter (i.e. with the divide-by-5 after the divide-by-2). Some slight modification may therefore be necessary.

Figure 9. Circuit for generating an alarm signal with variable pitch and rhythm.

Figure 10. Timing diagram for the circuit of figure 9, showing the tone sequences for the four possible states of A_4 and B_4.

Figure 11. Circuit to gradually increase the volume of the alarm signal if the sleeper does not awaken immediately.

Figure 12. A complete alarm circuit incorporating the ideas of the previous circuits.

Volume Control

In order not to awaken the sleeper too harshly it is a simple matter to arrange a volume control so that the alarm tone starts at a low level and gradually becomes louder and louder until it is switched off. This is achieved by the circuit of figure 11. The counter shown is the minutes counter (i.e. the one that drives the minutes display). Since the alarm can only be set in units of ten minutes, the alarm will sound when the tens of minutes have just changed to the required number and the minutes counter is reset. Outputs A to C of the minutes counter are thus at '0', so T2 to T4 are turned off. The alarm tone is applied to the base of T1 via R1 and switches this transistor on and off causing a signal from the loudspeaker. Since there is a 390 Ω resistor (R2) in series with it the tone is not very loud. After 1 minute the A output of the counter goes to '1', switching on T2 and thus connecting R3 in parallel with R2. The tone thus becomes louder. After 2 minutes output B becomes '1' while A becomes '0'. R4, which is smaller than R3, is paralleled with R2, so the tone becomes louder still. After 3 minutes outputs A and B are '1', and after 4 minutes output C becomes '1', by which time the tone is quite loud.

Output D is not connected to this system. If the sleeper has not awoken after 8 minutes output D will become '1' and can be connected to set off a small explosive charge underneath the bed. A less drastic cure for the deep sleeper is to connect an additional transistor to output D with a 56 Ω resistor in series with its emitter.

The complete circuit of an alarm system is given in figure 12. Everything within the dotted box is the alarm circuit, whilst everything outside is the existing clock circuitry. This differs slightly from the circuits discussed in that a HEX-inverter replaces the five-input NAND-gate in the alarm control circuit. This has open-collector outputs, so the outputs may be joined to perform a wired-OR function. In this circuit the additional transistor T9 is shown connected to output D5 for the extra loud alarm signal. A suitable printed circuit board and component layout for this alarm are given in figure 13.

The IC numbers shown in brackets in figure 12 correspond to those in the versatile digital clock.

Time Signal Generator

Provision of a 'six pips' time signal every hour is a relatively simple matter

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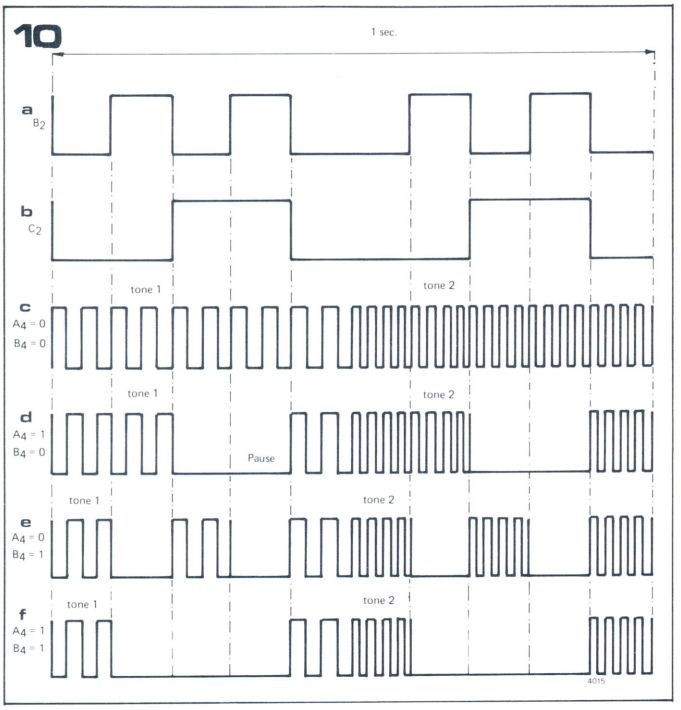

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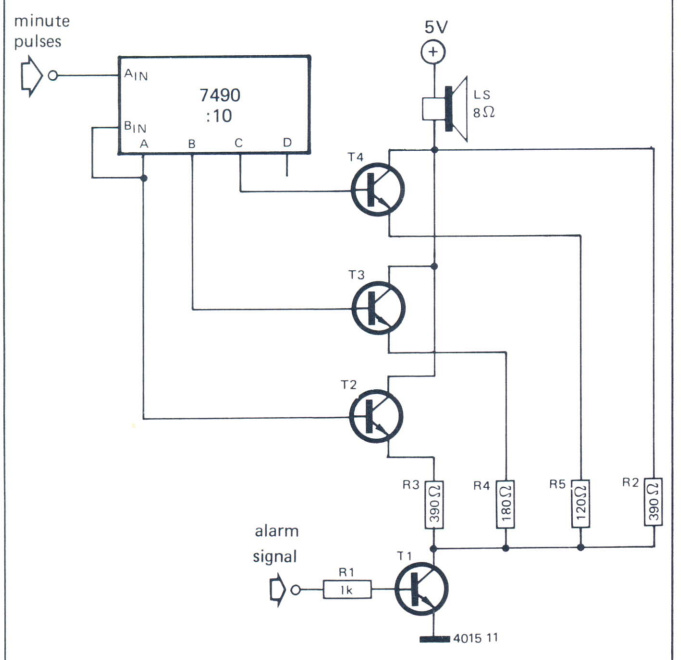

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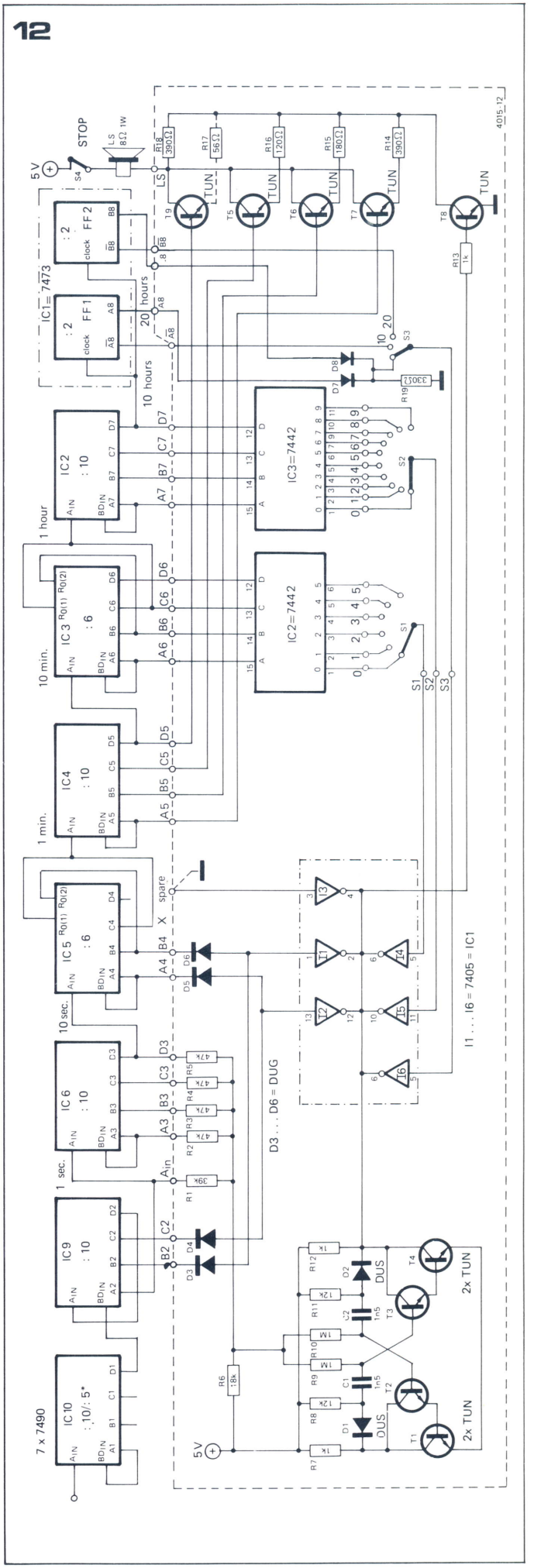


Components list for figure 12

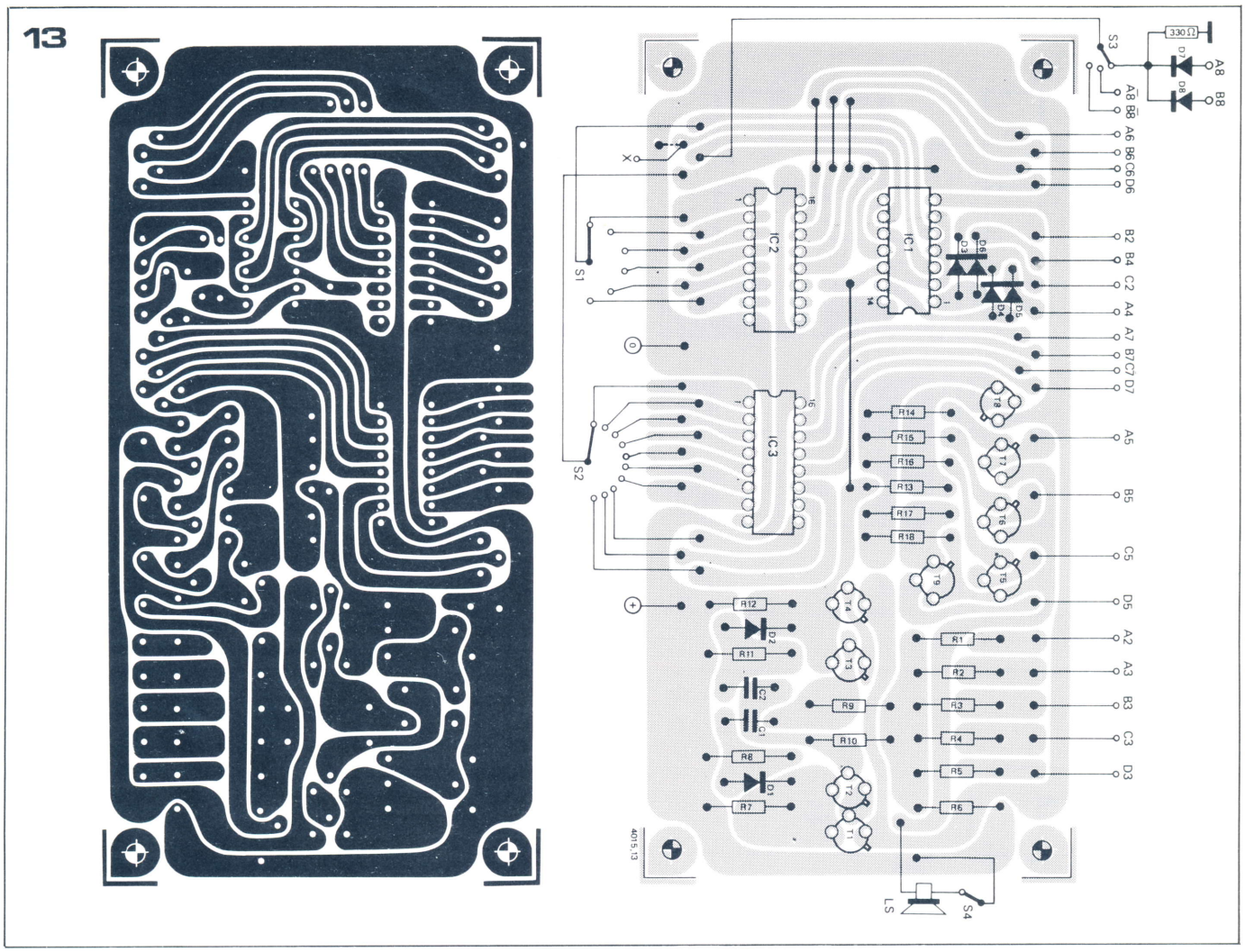
Resistors:
R1 = 39 k
R2 ... R5 = 47 k
R6 = 18 k
R7,R12,R13 = 1 k
R8,R11 = 12 k
R9,R10 = 1 M
R14,R18 = 390 Ω
R15 = 180 Ω
R16 = 120 Ω
R17 = 56 Ω
R19 = 330 Ω

Capacitors:
C1,C2 = 1n5

Semiconductors:
T1 ... T9 = TUN
D1,D2,D7,D8 = DUS
D3 ... D6 = DUG

IC's:
IC1 = 7401
IC2,IC3 = 7442

Switches:
S1 = single pole 6-way
S2 = single pole 10-way
S3 = single pole 3-way (decimal coded thumbwheel switches suggested)

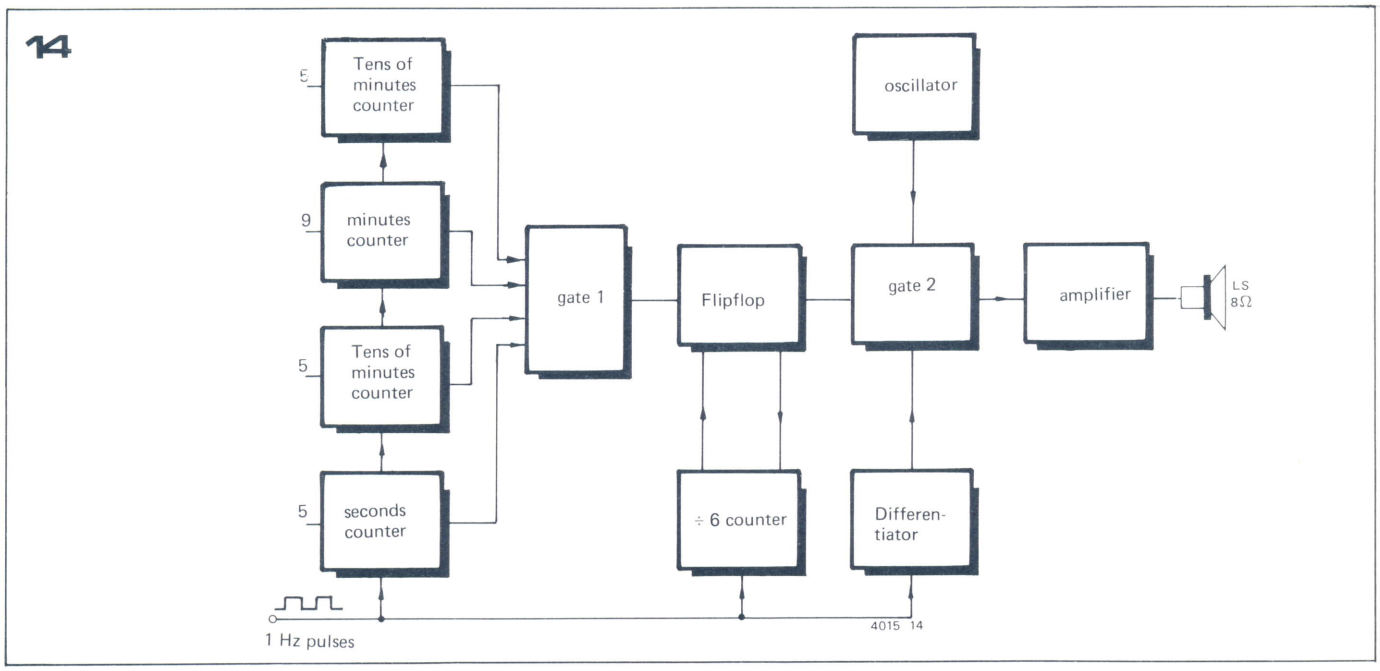


and a suitable circuit is given in figures 14 (block diagram) and 15. The portion of the circuit outside the dotted box in figure 15 is the existing seconds counter in the clock (IC6). The circuit works in the following manner:
the inputs of gate 1 are connected to the outputs of the tens of minutes, minutes, tens of seconds and seconds counters corresponding to the time 59 minutes 55 seconds. When this time is reached the inputs of gate 1 will all be high, so the output will be low. At any other time at least one input must be low, so the output will be high. Normally therefore, the $\overline{Q}$ output of IC2 is low, so the output of IC4b is high blocking the oscillator IC4a (which will be dealt with later), whilst the Q output is high, holding the ÷ 6 counter IC3 in

Figure 13. P.C. board and component layout for the circuit of figure 12.

Figure 14. Block diagram of a time-signal generator.

Figure 15. Complete circuit of the time-signal generator.



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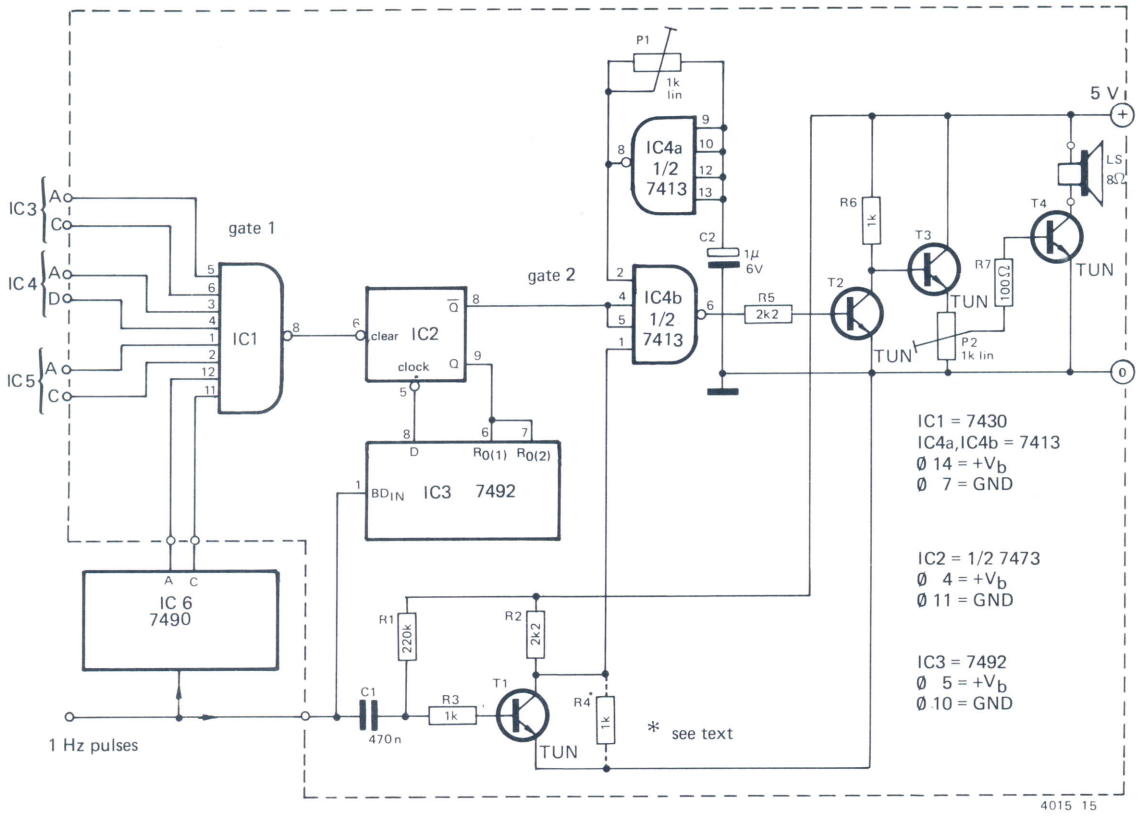


Components list for figure 15

Resistors:
R1 = 220 k
R2,R5 = 2k2
R3,R4,R6 = 1 k
R7 = 100 Ω
P1,P2 = 1 k

Capacitors:
C1 = 470 n
C2 = 1 µ, 6 V

Transistors:
T1 ... T4 = TUN

IC's:
IC1 = 7430
IC2 = 7473
IC3 = 7492
IC4 = 7413

the reset condition. On the negative-going edge of the incoming seconds pulse at 59 minutes 55 seconds the output of the seconds counter will assume the condition '5', i.e. outputs A and C high. The output of gate 1 will go low, clearing IC2 so that the Q output goes low and the $\overline{Q}$ output goes high.

IC3 may now count the incoming seconds pulses. However, due to the propagation delays through the seconds counter, IC1 and IC2, it will not count on the abovementioned negative-going edge, as this has already disappeared before the counter is enabled. However, the negative-going pulse is differentiated by C1 and R3 (neglecting R1 and the base resistance of T1), and turns off T1 for about 100 ms. This takes pin 1 of IC4 high, and since pins 4 and 5 are already held high by the $\overline{Q}$ output of IC2 the oscillator will be gated through it providing a 1 kHz tone burst of 100 ms duration.

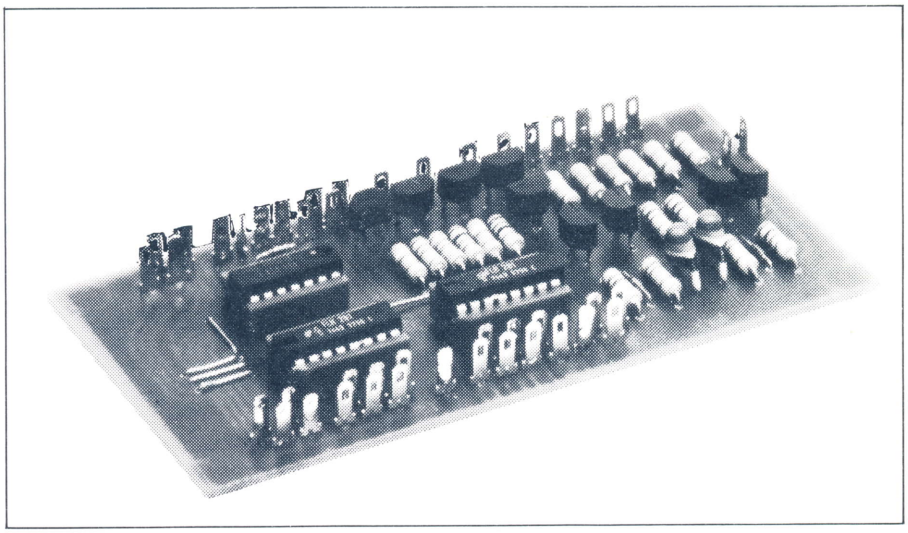
On each negative-going edge of the five subsequent second pulses IC3 will count and the oscillator will provide a 100 ms tone burst. On the fifth pulse the D output of IC3 will go high, and on the sixth pulse the D output goes low, clocking IC2, so that its Q output goes high and its $\overline{Q}$ output goes low. This disables the oscillator and holds the counter (IC3) in a reset condition so that it can count no further seconds pulses. This condition obtains for a further 59 minutes 55 seconds until it is time for the next signal. The circuit thus produces six pips every hour, starting with the first pip at 59 minutes 55 seconds and terminating with a pip exactly on the hour. Of course, this circuit produces pips of equal length, whereas the last pip of a radio time signal is longer than the preceding five. An alternative circuit, which produces this type of signal, is described elsewhere in this book.

Oscillator and Amplifier

The oscillator is a simple single time

COUNT	OUTPUTS D	C	B
0	0	0	0
1	0	0	1
2	0	1	0
3	1	0	0
4	1	0	1
5	1	1	0
0	0	0	0

Table II. Truth table for the 7492 connected as a divide-by-6 counter.



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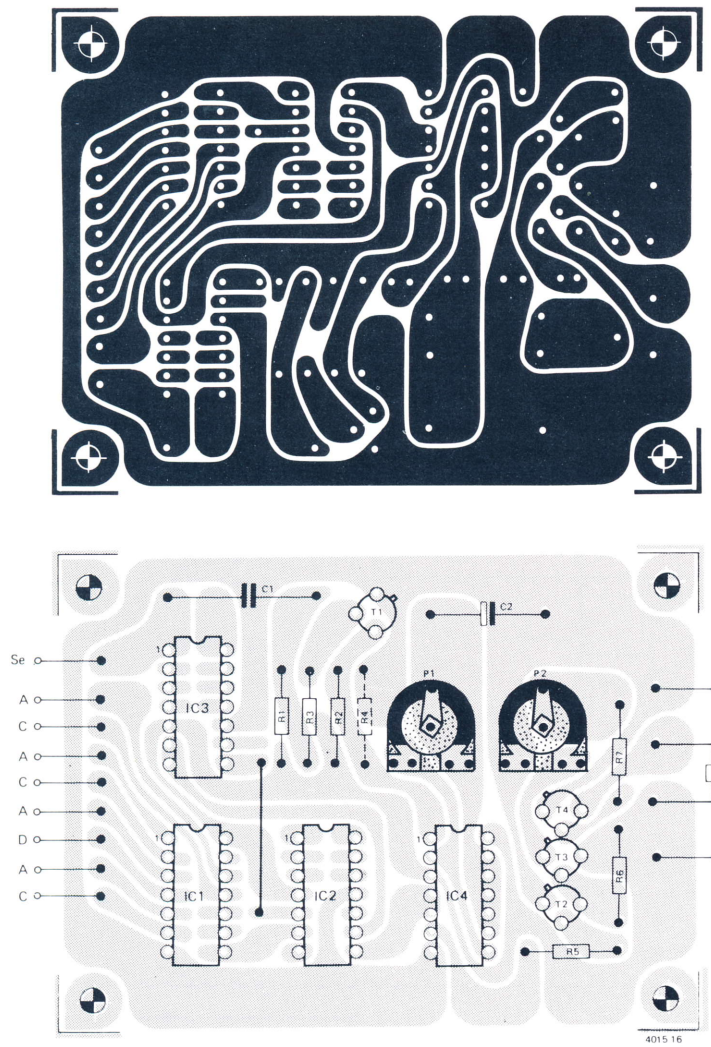
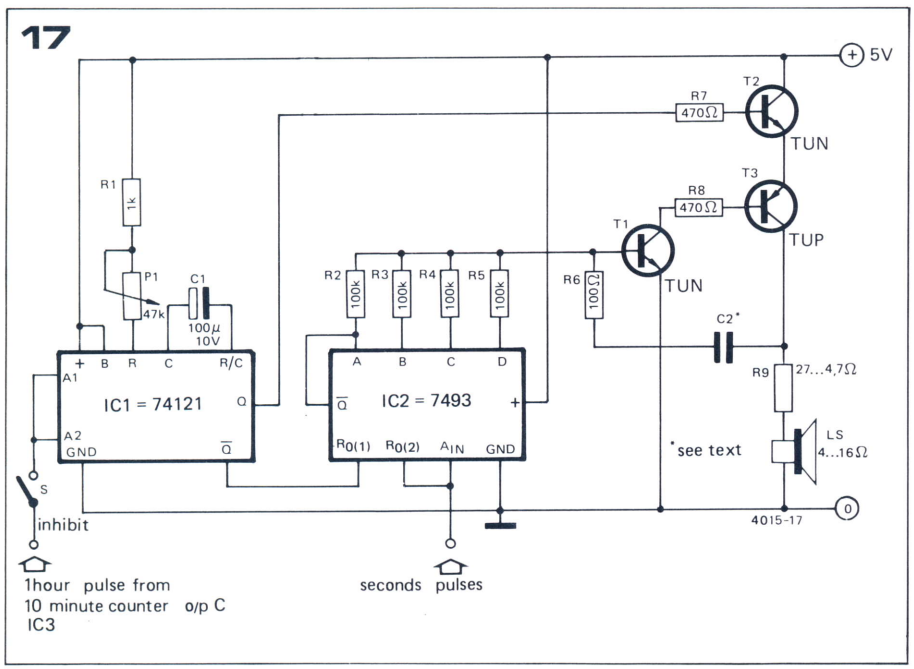


constant multivibrator based on the 7413 which is a dual 4-input NAND Schmitt Trigger. Assuming the output of IC4a is initially high then C2 will charge through P1 until the voltage across it reaches the threshold of the Schmitt trigger. The output will then go low and C2 will discharge through P1 until it falls below the threshold, when the output will go high again. Because of hysteresis the negative-going threshold is below the positive-going threshold, so the frequency of the oscillator is determined by the time taken to charge and discharge C2 between these points, which is of course dependent on the time constant P1C2. The oscillator frequency can therefore be varied by P1. With C2 = 1 μ and P1 set to 330 Ω the frequency will be about 1 kHz. Altering P1 also changes the mark-space ratio of the waveform, but this is unimportant in this application.

The other gate in IC4 is used to gate the oscillator output into the amplifier, consisting of T2 to T3. This is a simple switching amplifier, as only square waves are being dealt with. In the quiescent state only T2 is turned on so the current drawn is only about 7 mA.

17



P.C. Board

The track pattern and component layout of a board suitable for the time-signal circuit is given in figure 16. Note that R4 (shown dotted in figure 15) is a precaution against power supply ripple appearing at the loudspeaker output. Depending on the power supply it may or may not be necessary.

Chiming and striking systems

In a conventional chiming clock there are two systems. A chime, which plays a tune just before the hour, and a striking system, which sounds a bell a number of times equal to the number of hours. In more sophisticated clocks the chime may also play a portion of its tune at the quarter-, half- and three-quarter-hour marks. In simpler clocks the chime may be absent altogether. It is difficult to convincingly imitate bells and chimes electronically, so in this article two types of system are described, a fully electronic system driving a loudspeaker, and a hybrid electromechanical system suitable for driving a normal electric door chime.

The circuit of a simple electronic chime is given in figure 17.

It operates as follows:

every hour the tens of minutes counter in the clock produces a negative-going pulse that changes the state of the hours counter, and hence the hour display. In the circuit of figure 17 this is used to trigger a monostable with a period of about 4 seconds. The $\overline{Q}$ output of this monostable is connected to one of the reset inputs of a 7493 divide-by-16 counter, so that when the $\overline{Q}$ output of the monostable goes low the counter is enabled and counts pulses from the clock seconds counter, which are fed into the A input. T1 and T3 form a voltage-controlled oscillator, and as the output states of the 7493 change so does the voltage applied to the base of T1, thus altering the frequency of the oscillator.

The oscillator will thus produce a sequence of notes until the monostable resets, and when the seconds pulse input (which is also connected to the other reset input of the 7493) goes high then the counter will reset. T2, which is driven by the Q outputs of the monostable, switches the power supply to the

Figure 16. Board and component layout for the time-signal generator.

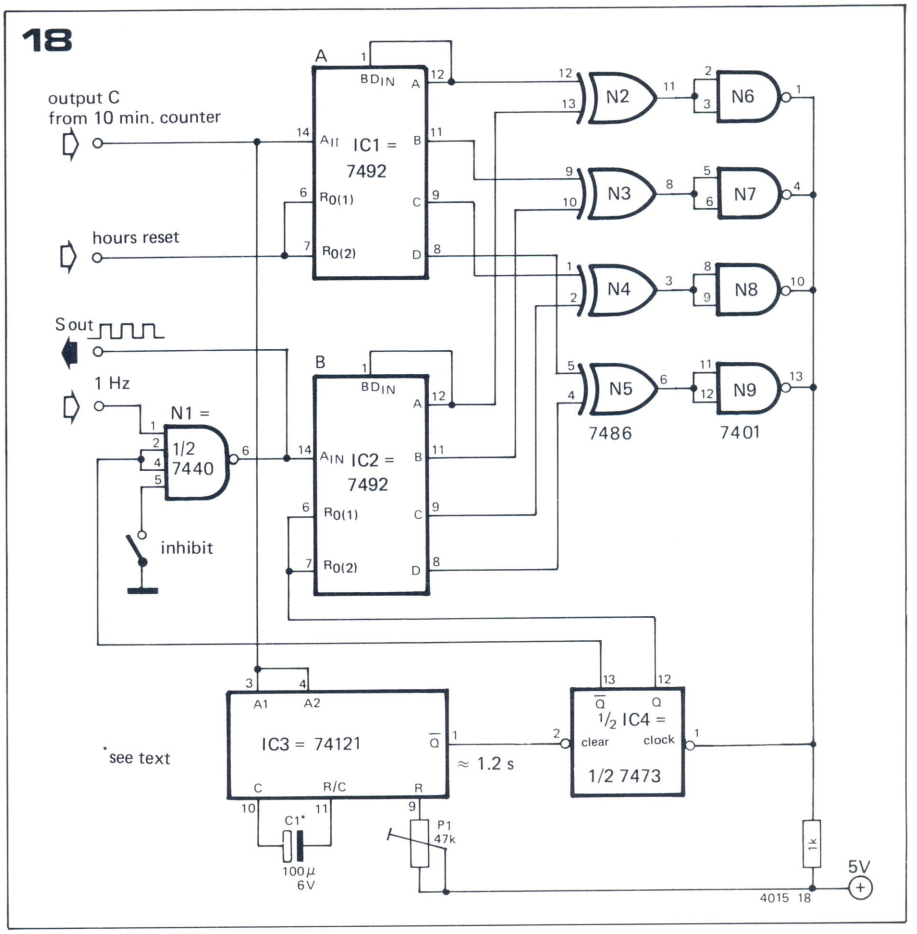
Figure 17. Circuit of a simple electronic chime.

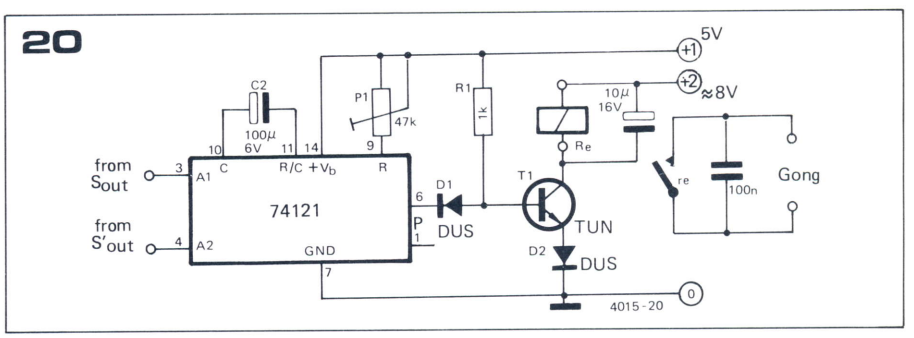
Figure 18. A striking system suitable for driving an electric bell or chime. P1 must be adjusted to give a monostable period time greater than 1 second but less then 2 seconds.

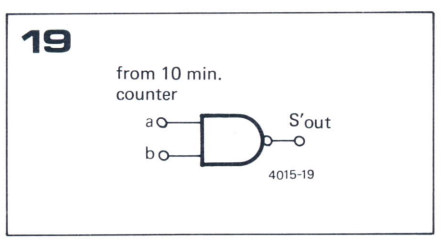
Figure 19. By gating the 3 output of the ten-minute counter and using it to drive the chime the clock will strike on the half-hours as well as the hours.

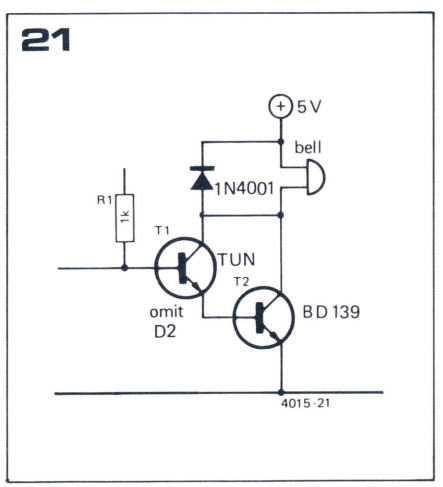
Figure 20. A suitable drive circuit to switch the chime. There are two inputs, one from the striking circuit and one from the half hour gating of figure 19.

Figure 21. If the drive circuit is used with a D.C. bell then the relay may be omitted and an additional transistor connected as shown will switch the bell.









VCO, thus disabling it when the chime has finished. P1 can be used to vary the length of the monostable pulse and hence the number of notes in the chime sequence. Altering C2 will change the frequency range of the VCO – the larger C2 the lower the frequency. As a final point, if a faster chime rate is required then the 7493 may be driven by 10 Hz pulses instead of 1 Hz pulses.

Striking the hours

A circuit for striking the hours is shown in figure 18. The basic idea is that the output of the hours counter is compared with the output of a second counter which is driven by 1 Hz pulses. Every hour on the hour 1 Hz pulses are gated into this counter until its count equals the output count of the hours counter. The number of 1 Hz pulses required to achieve this state is thus equal to the number of hours and these pulses may be used to drive a chime or bell.

The circuit operates in the following manner: instead of using the hours counter in the clock to provide the required information an auxiliary divide-by-12 counter (IC1) is used. This has the advantage that (coded) outputs from 0 - 11 are available directly from a single counter, whereas deriving these outputs from the hour and ten-hour counters in the clock would require additional gating. It should be noted that, whereas the clock counts hours 1-12 the counter counts 0-11. This is no disadvantage as there are still 12 output states for the striking system.

Every hour on the hour monostable IC3 is triggered by the output of the ten-minute counter. The $\overline{Q}$ output of this monostable is used to clear flip-flop IC4, thus allowing 1 Hz pulses from the seconds counter through N1. IC2 now counts the 1 Hz pulses. Exclusive-OR gates N2 - N5 are used to compare each bit of the hours count with each bit of the output of IC2. When each bit is equal the outputs of N2 - N5 are all low so the commoned outputs of N6 - N9 go high. On the next pulse to IC2 the outputs of the two counters become different and the commoned outputs of N6 - N9 go low again, thus clocking IC4.

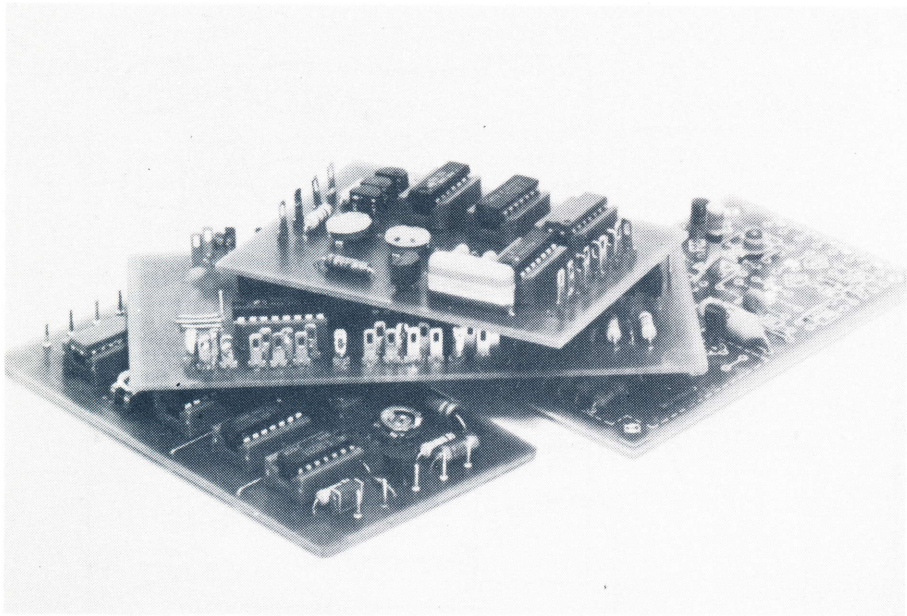


Figure 22. Circuit of a complete striking system. P1 must be adjusted to give a monostable period time greater than 2 but less than 4 seconds.

Figure 23. Printed circuit board and component layout for the striking system of figure 22.

The Q output of IC4 goes high, resetting IC2, while the $\overline{Q}$ output goes low, blocking N1 so that no more 1 Hz pulses can be counted. The number of pulses allowed through N1 is thus equal to the count of IC1 plus 1, which is of course the number of hours since IC1 is always one digit behind the counters in the clock. The pulses can therefore be taken from the output of N1 and be used to drive the chime or bell.

To ensure that counter IC1 is in synchronism with the clock hours counters, and thus prevent the wrong hour from being struck, it is necessary to

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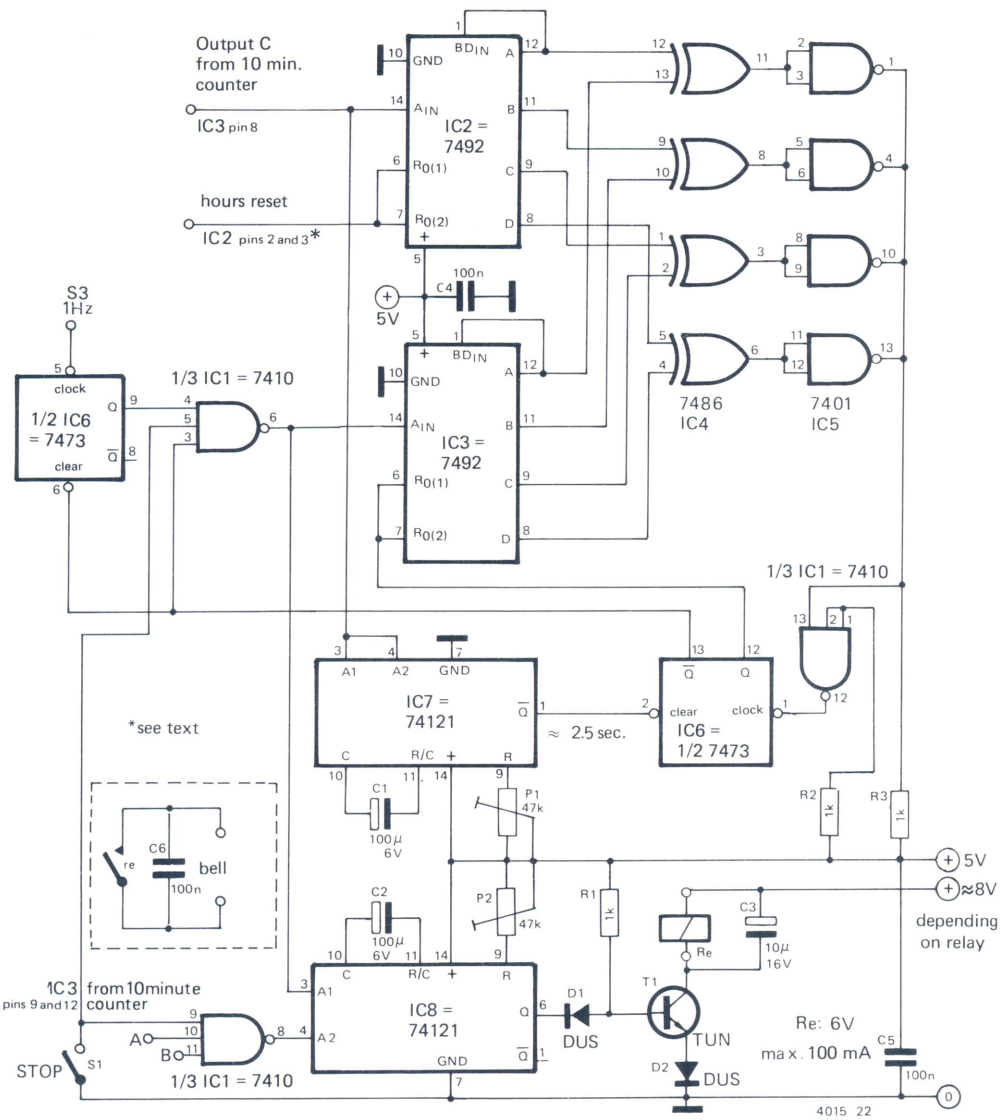
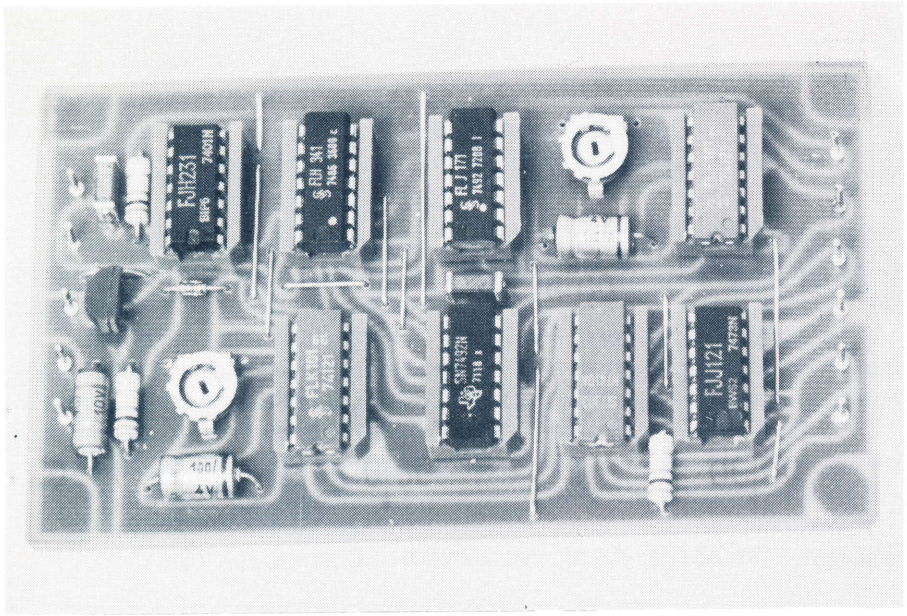




reset IC1 to zero at the change from 12 to 1 o' clock in a 12 hour system, or at the transition from 12 to 13 hours or 00 to 01 hours when used with a 24-hour clock.

Striking the half-hour

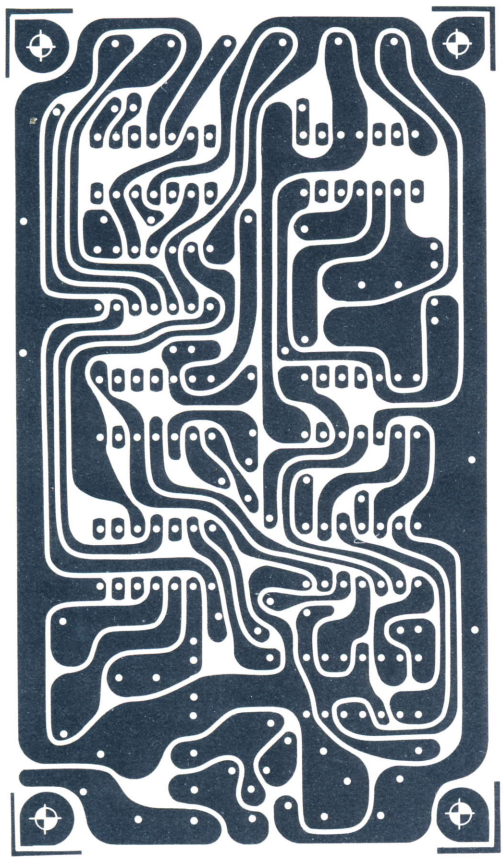
As a small refinement it is possible to make the clock strike once on the half-hour. As the half-hour corresponds to an output of 3 or binary 0011 on the tens of minutes counter this can easily be derived by NANDing together the A and B outputs of the ten-minute counter in the clock, as in figure 19. The output of this NAND-gate can then be used to trigger the bell, which will then strike every half-hour.

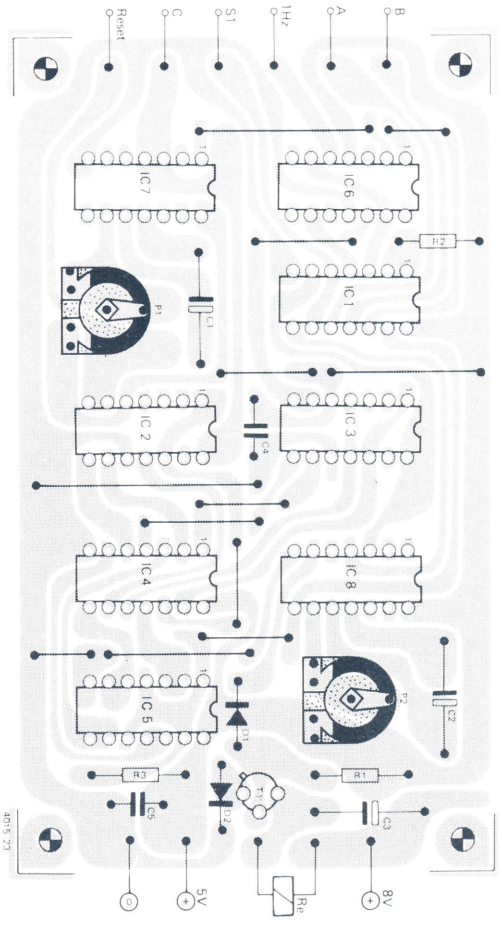
A suitable drive circuit for the bell is given in figure 20. It consists of a monostable multivibrator driving a transistor which switches a relay. This enables the circuit to be wired into the household A.C. doorbell circuit. If a separate (D.C.) bell or chime is used it is possible to drive it directly with a transistor and dispense with the relay, as in figure 21. P1 adjusts the pulse length of the monostable and hence the time for which the bell coil is energised. It should be adjusted so that the bell will just strike reliably, to minimise the energised time and hence the dissipation in the coil. If a normal ding-dong type of door chime is used it may be a good idea to remove one of the tubular or bar resonators so that the chime produces only a single stroke. In the larger tubular type of chime the tubes are usually suspended on cord or wire and are easily removed. The smaller types of chime usually employ metal bar resonators which are suspended from rubber mounts. These can also be removed quite easily.

The circuit of a complete striking system is given in figure 22. It embodies the ideas of figure 18 together with the half-hour striking circuit of figure 19. The only difference is that the spare half of IC6 is utilised and the striking occurs at a ½ Hz rate. If this is thought to be too leisurely then the seconds input can be connected direct to pin 4 of IC1. A printed circuit board and component layout for this circuit are given in figure 23.

The connections to the 'versatile clock' are shown in brackets in figure 22. Note that two hours reset lines are required, so the connection between pin 6 and 7 of IC2 in figure 23 must be broken, after which these two pins are pairwise connected to pins 2 and 3 of IC2 in the clock.

23

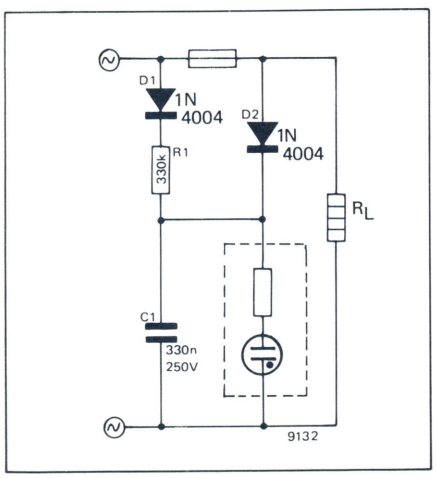




J.W. van Beek

fuse indicator

In this circuit, the neon indicator lamp shows whether or not the power is on and whether or not the fuse is blown.
As long as the power is on and the fuse is intact, the neon lamp will draw current through the fuse, D2 and the built-in series resistor. It will burn brightly to indicate that all is well.
If the fuse is blown, however, current can only flow through D1 and R1. This current will charge C1 until the ignition voltage of the neon lamp is reached. The lamp will light up. It will now draw enough current to discharge C1 until the extinction voltage is reached, whereupon the lamp will go out again. C1 recharges through R1, and the cycle repeats. The result is that the neon lamp will flash continuously as long as the power is on.
The only critical points in this circuit are the resistors. The value of R1 must be so large that current flowing through this resistor into the neon lamp is insufficient to keep it ignited. On the other hand, the built-in resistor should be small enough to discharge C1 fairly rapidly but not so small that the lamp will 'burn out' when fed directly through D2 (actually, a neon lamp doesn't burn out - it can progressively darken as the electrode material 'migrates' to the inside of the glass envelope).



disc preamp

A preamplifier-equaliser for magnetic pickup cartridges has to meet quite exacting requirements. Values for gain, noise level and maximum input voltage which will guarantee trouble-free operation under all conditions are not so easy to achieve. The well-known two-transistor configuration, operating from a 12 . . . 18 V supply, invariably falls short on gain and overdrive-margin - unless it is designed for a low nominal output voltage (about 30 mV). An alternative approach is to make use of a good integrated amplifier. The design about to be described, which meets all the requirements, employs a SN 76131. An almost identical I.C. is the μA 739.

To make optimum use of the possibilities for groove-modulation, gramophone records are cut with low audio frequencies attenuated and high audio frequencies boosted (with respect to 1 kHz). To simplify playback equalisation, a single weighting curve has been standardised throughout the world - the IEC disc-cutting characteristic. (This curve originated as the RIAA standard: Record Industry Association of America).
The disc-cutting engineer arranges for a '0 dB standard (reference)level' in the taped programme to produce a stylus tip-velocity about 14 dB below the 'safe' drive-level, to provide headroom for instantaneous signal peaks. 0 dB standard level (corresponding roughly to the average level in loud passages) is typically 39 mm/sec tip peak velocity at 1 kHz. Standard level on carrier-channel discs (CD4 and UD4) is lower, about 22 mm/s.

Experience indicates that wide-band cartridges suitable for carrier discs deliver 70 . . . 140 μV for each mm/sec of tip velocity. The usual 'hifi' cartridges deliver about 6 dB more. (Note that sensitivity specifications are usually given in RMS millivolts per peak centimetre per second). So the input to the preamplifier at standard level 1 KHz will be about 1 . . . 10 mV peak.
What are the consequences of all this for the preamplifier?

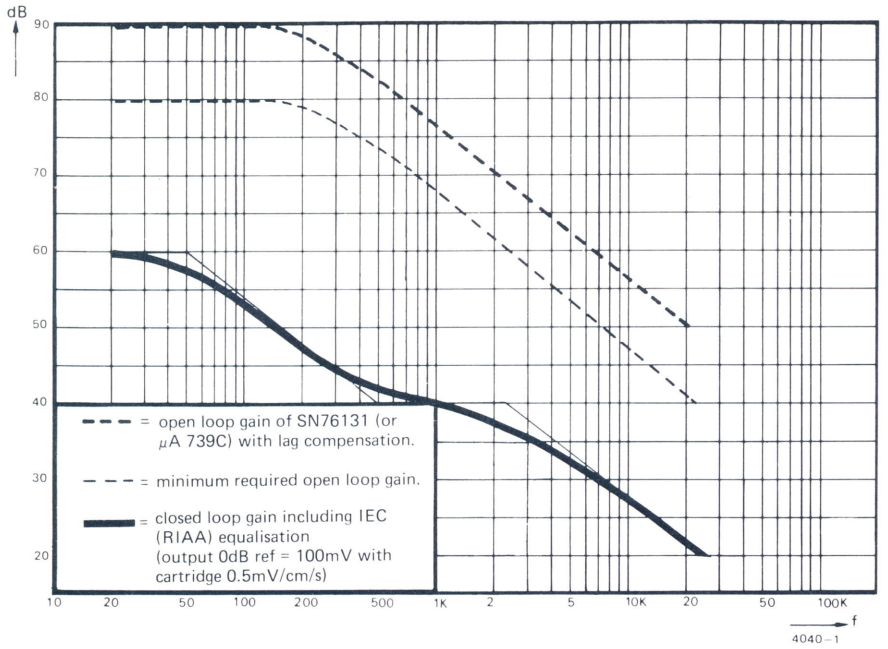
Suppose it is the intention that the output voltage at standard level be about 100 mV RMS with the lowest-output cartridge. The closed-loop gain must therefore be 100 at 1 KHz. Now allow 20 dB of extra gain for IEC equalisation at the lowest frequencies, not including 20 dB of negative feedback (which should reasonably be maintained at the 'low end'). This tots up to an open-loop gain of at least 80 dB! Ten thousand times. That seems to eliminate the two-transistor configuration.
The SN 76131 integrated circuit, with the chosen lag compensation, has a typical open-loop response according to the upper dashed curve in figure 1. The

Figure 1. The desired closed-loop gain curve follows the IEC (RIAA) disc equalisation characteristic, with a mid-band gain (1 KHz) of 40 dB (heavy line). The open-loop gain must be at least 20 dB greater; the SN 76131, with the chosen lag compensation, provides this with a margin of about 10 dB (upper dashed curve).

Figure 2. The heavy line is an estimated contour for the highest voltage delivered to the preamplifier by a high-output dynamic cartridge. The preamplifier cannot be overdriven by the highest input voltage; the upper dashed line is the overdrive threshold for the disc-preamplifier with SN 76131. This clears the maximum-input contour by approximately 10 dB.

Figure 3. The maximum RMS output level produced by the preamp when used with a high-output cartridge follows the thick contour. The dashed line indicates the maximum output capability. The safety margin is here once again about 10 dB.

1



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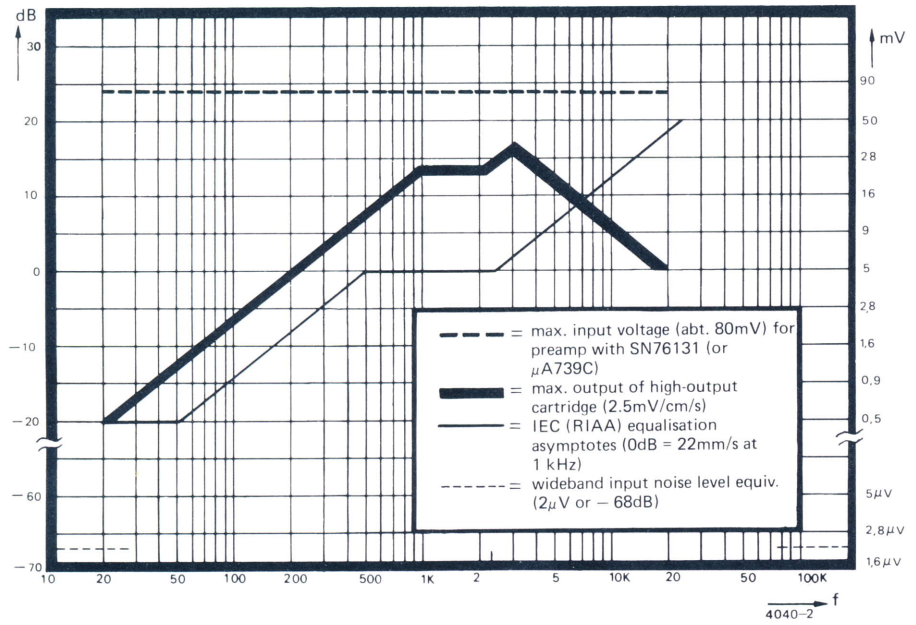

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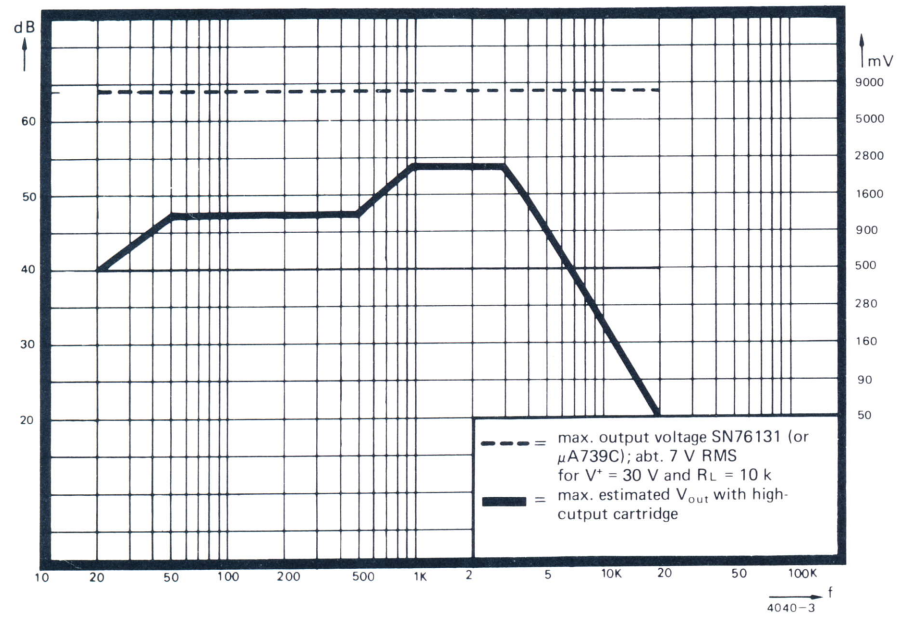


lower dashed curve indicates the minimum requirement (80 dB at the low end, reducing as the closed-loop gain – i.e. the bold line in figure 1 – falls according to the IEC curve). The conclusion is that there is about 10 dB of open-loop gain to spare at all frequencies, which will accomodate IC-tolerances etc.

Overdriving the input

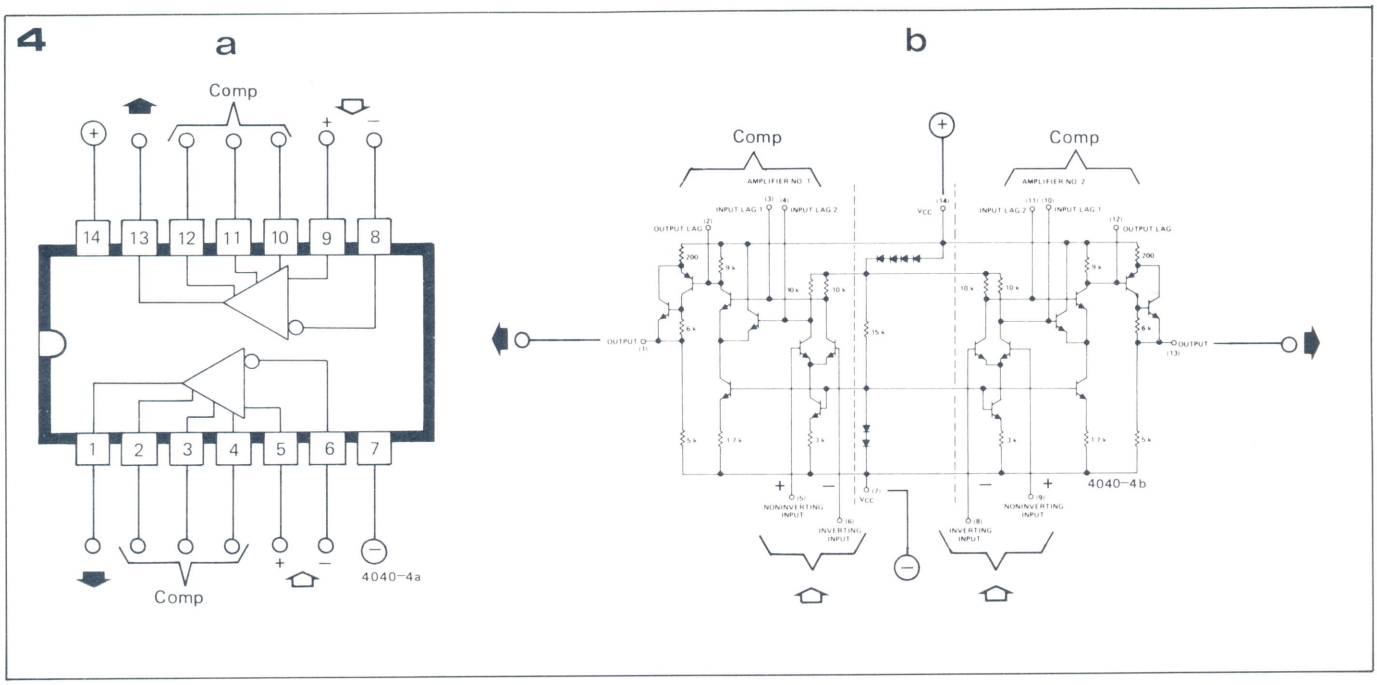
To find the maximum input voltage which can occur, one must start with the highest-output cartridge. This will deliver, as shown earlier, about 5 . . . 10 mV peak at standard level.

The maximum level encountered on the disc is nominally +14 dB relative to standard level. This indicates a nominal maximum input voltage of 25 . . . 50 mV. (At 1 KHz of course). It is clearly advisable to regard this figure, with due respect, as nominal. One might encounter a cartridge with still higher output or some disc manufacturer may fully exploit tracing-compensation, to cut a clean signal at more than +14 dB . . . The absolute limit (set by 'slope-overload' at the inner radius of LP discs) is presently about 350 mm/s (+18 dB) – but a 33 disc also has outer grooves and they can be cut at a level 6 dB higher. This means that in theory the maximum output level for the highest output cartridge is about 200 mV! With the circuit arrangement given, the SN 76131 will accept 80 mV at the input (thick dashed line in figure 2).

The same figure can be used to estimate the effect of amplifier noise. The wide-band noise level, referred to the SN 76131 input, is 2 μV (RMS). This is –68 dB in the figure (0 dB = 5 mV RMS). For the least sensitive cartridge, this noise level is –54 dB relative to standard level for CD-4 or UD-4 discs. Assuming maximum signal level to be +14 dB the overall S/N ratio is (for this worst case) 68 dB. Manufacturers estimate that the S/N ratio possible with a first-rate LP pressing is about 70 dB. Conclusion: pass.

Figure 2 can be used once more to determine the hum-level requirements. The IEC bass-lift now aggravates matters: to achieve a hum level 60 dB below standard level, with a fairly high-output cartridge (5 mV RMS at 1 KHz), it becomes necessary to keep the hum voltage at the input below 1 μV! This can be achieved, in general, by providing good screening for the input circuit and for the preamplifier itself (signal-return inside the cable-screen, the latter bonded to signal-earth at the amplifier end only), and by properly smoothing (preferably regulating) the DC supply.

The sensitivity of the SN 76131 to interference on the DC supply rail is quoted – under operating conditions rather different to the above – as 50 μV/V. (i.e. 50 μV apparent input for each volt of supply disturbance). To achieve the 1 μV hum level just mentioned means keeping supply ripple below 20 mV. A simple active circuit will readily meet this requirement;



simple smoothing of a 'raw' DC supply would probably be inadequate or too expensive (or both!).

Clipping at the output

The requirement that the input circuit is not overdriven will not by itself quarantee that the amplifier as a whole operates within limits. The output circuit can still 'run out of' voltage or current swing.

Taking the combination of a sensitive cartridge and the maximum disc modulation likely to be encountered, one can estimate the highest level of output signal that the preamplifier will have to deliver. This can be done by combining the closed-loop gain characteristic (figure 1, thick line) with the maximum cartridge output contour (thick line in figure 2). The result is shown in figure 3 (thick line). The conclusion is that the voltage swing at the output can be as high as 2.5 V RMS (7 V p-p).

The clipping level for the SN 76131 depends on the supply voltage and on the load impedance. The case of $V^+ = 30$ and $R_L = 10$ K, where the IC can deliver about 7 V RMS, is shown dashed in figure 3. This reserve should take care of all eventualities. If one considers a brink-of-disaster capability of 3 V RMS, then the combinations 18 V/5 K, 14 V/10 K and even $V^+ = 12$ (at $R_L = 50$ K) are in order. Even under these conditions, current clipping due to the load of the feedback network on the output (at the highest audio frequencies) and slew-rate limiting (due to the early open-loop rolloff) are not expected to occur.

Integrated circuit

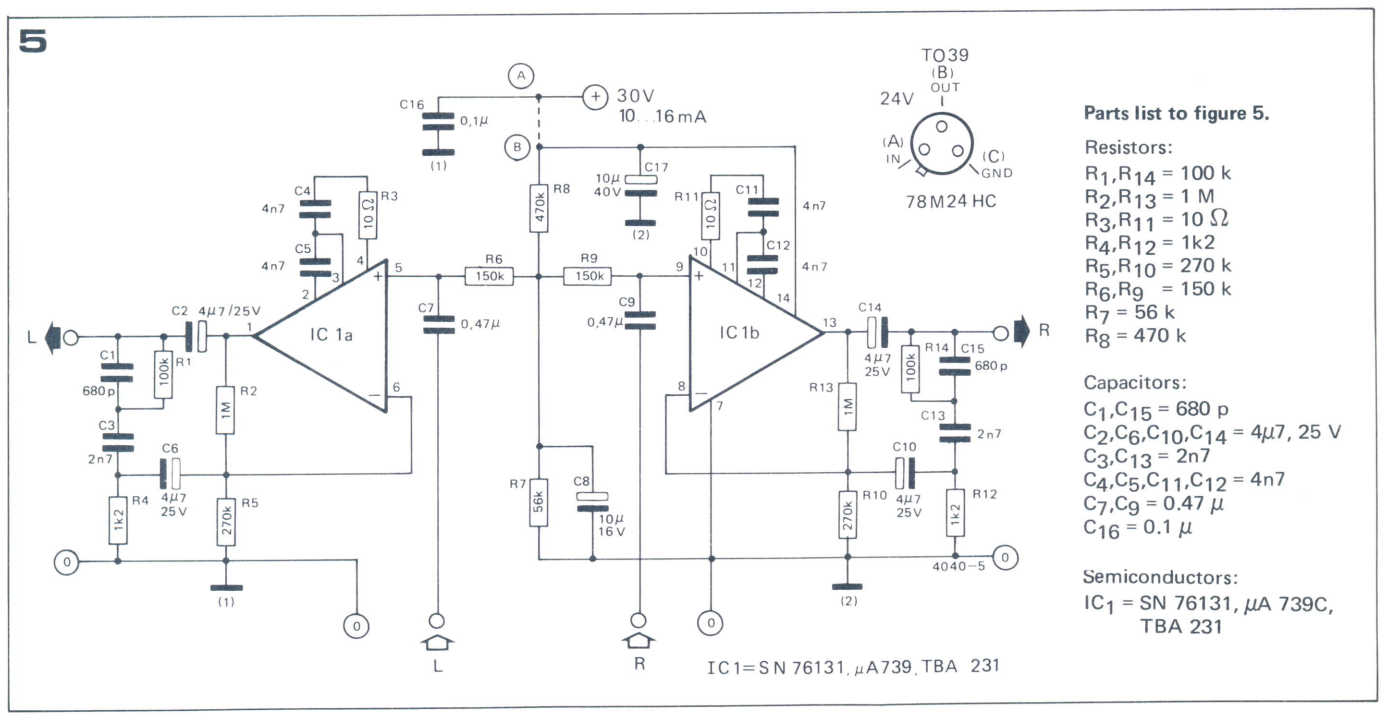
The circuit was designed around the specified SN 76131 by Texas Instru-

Figure 4. The pinning of the IC's SN 76131, TBA 231, TCA 590C, μA 739C and LM 1303 (figure 4a) is identical. The internal circuit diagram (figure 4b) however only applies to the SN 76131.

Figure 5. The circuit diagram of the equaliser-preamplifier. An integrated voltage regulator, when required, can be connected between the points A and B (see text).

Figure 6. PC board and component layouts for the equaliser-preamplifier. All external connections are made to one edge of the PC board, so that it can be used as plug-in module in a complete control amplifier.

Figure 7. Illustration of the preamplifier board as plug-in module.



Parts list to figure 5.

Resistors:
R_1, R_{14} = 100 k
R_2, R_{13} = 1 M
R_3, R_{11} = 10 Ω
R_4, R_{12} = 1k2
R_5, R_{10} = 270 k
R_6, R_9 = 150 k
R_7 = 56 k
R_8 = 470 k

Capacitors:
C_1, C_{15} = 680 p
C_2, C_6, C_{10}, C_{14} = 4μ7, 25 V
C_3, C_{13} = 2n7
C_4, C_5, C_{11}, C_{12} = 4n7
C_7, C_9 = 0.47 μ
C_{16} = 0.1 μ

Semiconductors:
IC_1 = SN 76131, μA 739C, TBA 231

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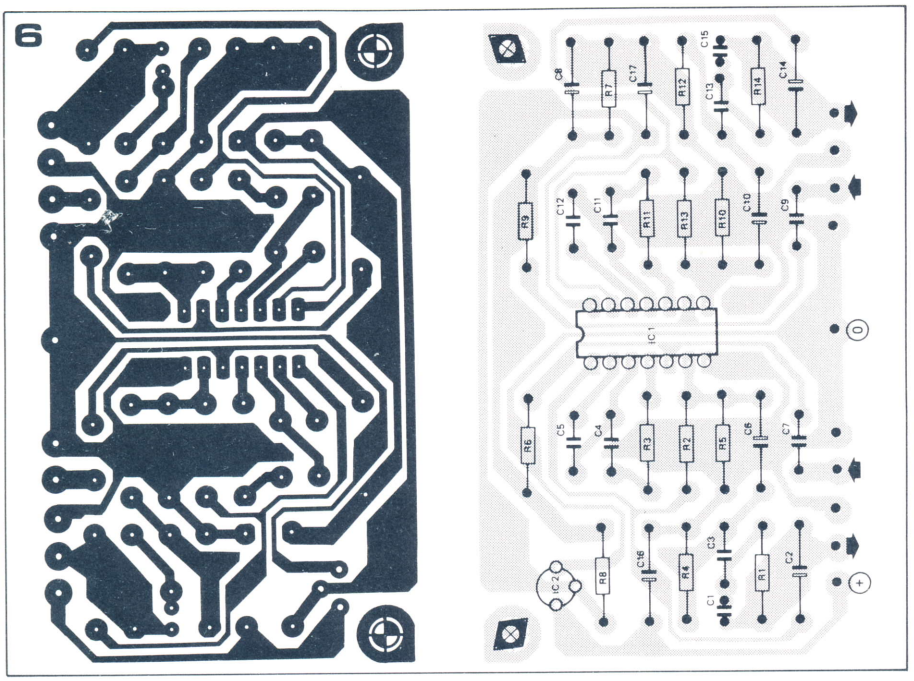

Table 1. The most important specifications of the SN 76131 and μA 739C.

V^+ max.	36 V
V_{in} max.	±5 V
P_{tot} max.	500 mW
V_{out} swing	1 . . . 26 V*
Open loop gain typ	18000*
Open loop gain min	6500*
Z_{in} typ.	150 KΩ*
Z_{in} min.	37 KΩ*
Z_{out} (1 KHz)	5 KΩ*
Crosstalk (10 KHz)	−140 dB*

* These values apply for V^+ = 30 V; R_L = 50 KΩ

Table 2. Main specifications of the disc preamplifier described here.

Voltage gain, 1 KHz	40 dB
Equalisation IEC	±1 dB
Max. input (RMS)	80 mV
Max. output (RMS)	7 V
Input noise level	2 μV
S/N ratio	55 . . . 70 dB*
Crosstalk (1 KHz)	−80 dB
T.H.D.	⩽0.1%

* see text

ments. According to the maker's data sheets, the Fairchild μA 739C and the SGS TBA 231 are almost identical and should perform well in the circuit. The three IC's are pin compatible (see figure 4a). Two other IC's with the same pinning are the Philips TCA 590 C and the LM 1303 by National Semiconductors. This last device has lower specifications for gain, noise and drive level – it will probably work acceptably in the preamplifier, but we have not checked this.

The internal circuit of the SN 76131 (and the TBA 231) is given in figure 4b. Except for the output transistor, the μA 739C is identical. Table 1 lists the most important characteristics of the device. The TCA 590C has an additional class B output stage, while the LM 1303 circuit dispenses with the stabilising diodes and with the current sinks for the second long-tail pairs.

The external circuit

Figure 5 gives the complete circuit diagram of the equaliser-preamplifier. The open-loop response is set up by $C_4/C_5/R_3$ and $C_{11}/C_{12}/R_{11}$; it follows the appropriate dashed curve in figure 1. The IEC correction networks are $R_1/R_2/R_4/C_1/C_3$ and $R_{12}/R_{13}/R_{14}/C_{13}/C_{15}$. R_5 and R_{10} take care of the DC biassing. With the values given, the correction obtained using 5% components is within 1 dB of the IEC (RIAA) standard.

The input blocking capacitors C_7 and C_9 should not be replaced by larger values or by electrolytics. This could lead to undesirable switch-on phenomena ('plop' or even momentary oscillation). The values given will not affect the bass response (which is 1 dB down at 20 Hz).

It has already been pointed out that the supply ripple must be well filtered. A typical regulated supply will meet the requirements, but a 'raw' supply followed by resistor-electrolytic filter will usually cause too much hum. In this case one can use an IC voltage regulator which will deliver 24 . . . 30 V at 15 mA (or more), e.g. the Fairchild μA 78M24HC. The printed circuit board (figure 6) has a position for this regulator. If such a device is not to be used, the points A and B should be bridged.

To simplify assembly, all external connections have been placed at one edge of the PC board, using standard grid-spacing. This means that it is possible to mount the disc preamplifier as a plug-in module on a suitably designed control amplifier board (figure 7).

Table 2, in conclusion, summarises the most important specifications of the equaliser-preamplifier for disc records.

Lit.: Texas Instruments data sheets for SN 76131.

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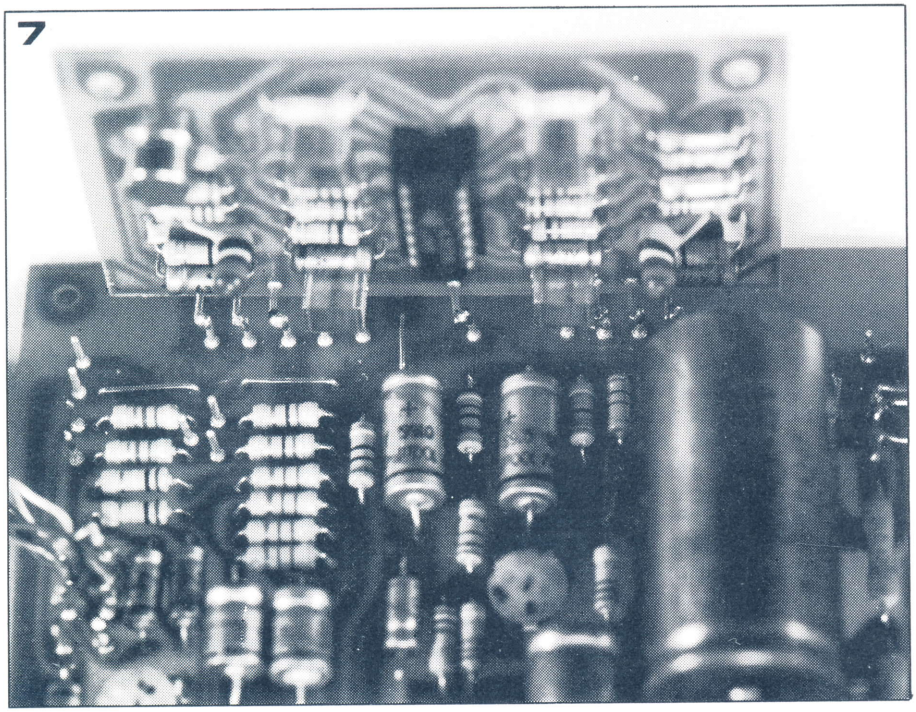
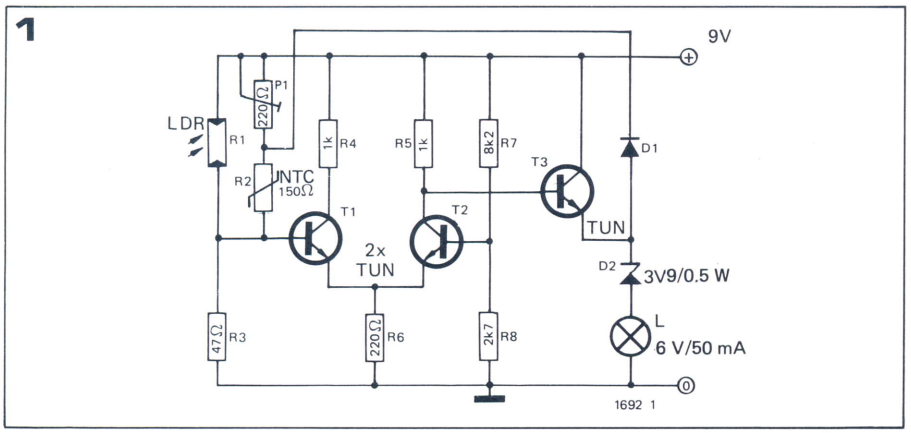


electronic candle

The starting point for design of this electronic candle was a desire to reduce the fire risk associated with the Christmas season, at the same time providing a candle which would not burn up so quickly. Naturally, the electronic candle can be lit with a match (but a pocket torch will do the job too!); it can be blown out or 'nipped out' with the fingers.



The circuit is very simple. In the condition 'candle out' no current flows in T1 and T2 is saturated. A certain pre-heat current is passed through the NTC-resistor (R2) via P1. This trimmer has to be adjusted so that the candle is just not 'self-igniting'. Strong illumination of the LDR (R1) will cause T1 to conduct. The circuit is arranged so that even bright room lighting will not cause things to happen – a burning match held close to the LDR will however do the trick nicely.

When T1 starts to conduct, the current through T2 is reduced until ultimately this transistor cuts off. T3 will meantime start to conduct, lighting the candle flame. As T3 approaches saturation an extra heating current flows via D1 into the NTC, causing this to drop in resistance value. If the match is held long enough in position – it should almost burn down to the fingers – the circuit will hold in the 'candle lit' condition.

The candle can be blown out if one blows long and hard enough on the NTC. The ultra-slow triggering action of starting up is now reversed and the lamp-current falls away to zero – the flame goes out. It is also possible to 'nip out' the candle by cooling the NTC between two fingers. The prototype candle used a miniature NTC having a resistance at room temperature of about 150 ohm.

If desired, one can replace the zener-diode D2 by 5 series-connected DUS universal diodes.

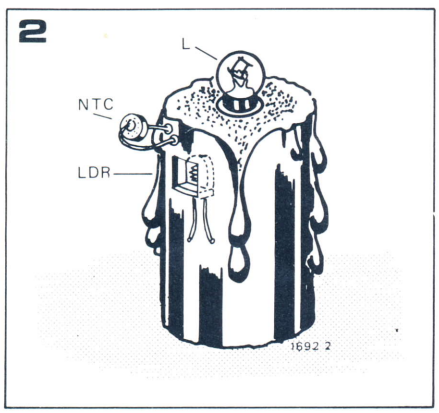


Figure 1. Circuit diagram for the 'electronic candle'. P1 is adjusted so that the lamp just does not light up spontaneously. The candle is 'lit' by holding a match (or a torch) close to the LDR, and 'put out' by blowing on the NTC.

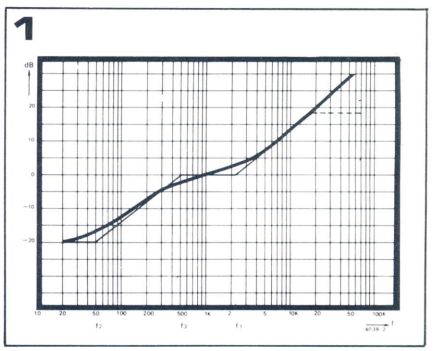
Figure 2. A sketch of one possible construction method. The candle is made from a piece of PVC electric-wiring conduit.

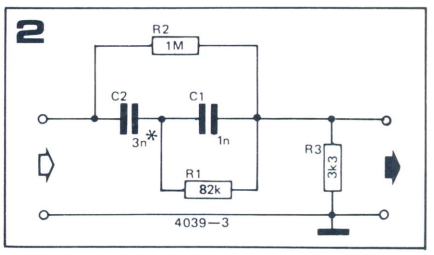
recip-riaa

The performance of bought or self-built preamplifiers for magnetic pickup cartridges is invariably not sufficiently well known. This is mainly due to the

Carrying out measurement on a disc-preamplifier involves two specific, normally time-consuming complications. First of all, one cannot straightforwardly check the frequency response; carrying out such a check on the dynamic preamplifier requires a point-by-point comparison of the meter reading with a voltage-frequency table.

This brings us to the second complication. A correct test of the nominal or maximum available output voltage as a function of frequency is only obtained when the input voltage follows the weighting curve used during cutting (figure 1). The simple and direct solution





Performance characteristics of the weighting network. Noise and distortion levels will in practice be those of the LF oscillator in use.

Maximum amplitude error with 1% components	± 0,2 dB
Maximum amplitude error with 5% components	± 0.9 dB

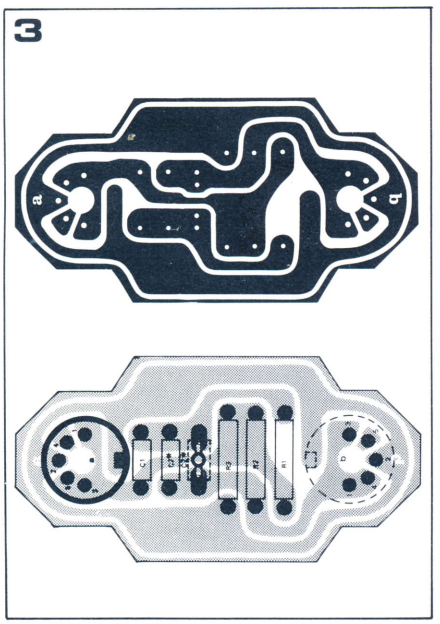
work involved in accurately measuring the amplitude response (RIAA or IEC curve), overdrive margin, distortion, signal-to-noise ratio and hum level. The weighting network described here greatly simplifies the above-mentioned measurements. Despite its simplicity, using only five components, it will deliver a measurement signal that is within 0.2 dB of the standard RIAA cutting-curve. This should make it just about the smallest professional test instrument ever described . . .

to both problems should now be obvious: insert a weighting network having the amplitude-frequency response of figure 1 between the constant-voltage oscillator and the preamplifier under test. A suitable network is shown in figure 2.

Figure 1. The IEC/RIAA weighting curve used during disc cutting. The 'recip-RIAA' network also produces this curve.

Figure 2. Circuit diagram of the network. C2 can be made up by parallel connection of twice 1.5 nF (or 2.2 nF plus 820 pF).

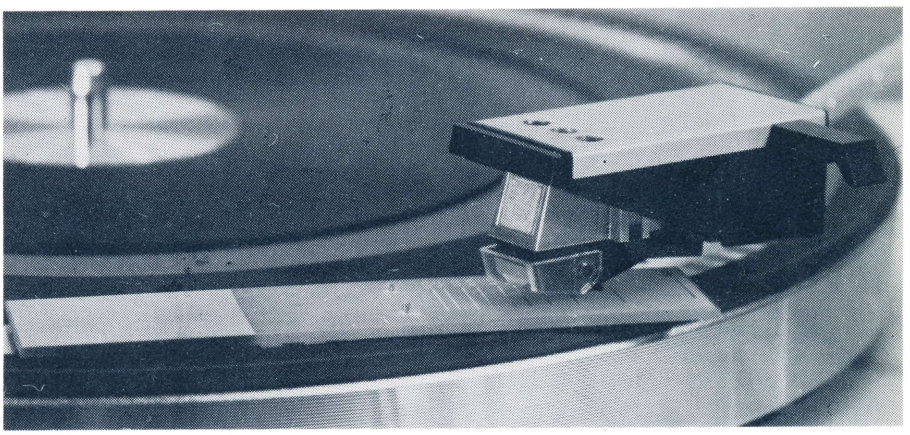
Figure 3. PC board and component layout for the network (EPS 4039).



Signal-to-noise ratio	80 ... 120 dB
Distortion (with film resistors)	below noise
Oscillator output voltage for routine testing (0 dB = ± 3.5 mV at 1 kHz)	100 mV
Oscillator output voltage for overdrive test (+26 dB)	2 V

Stylus balance

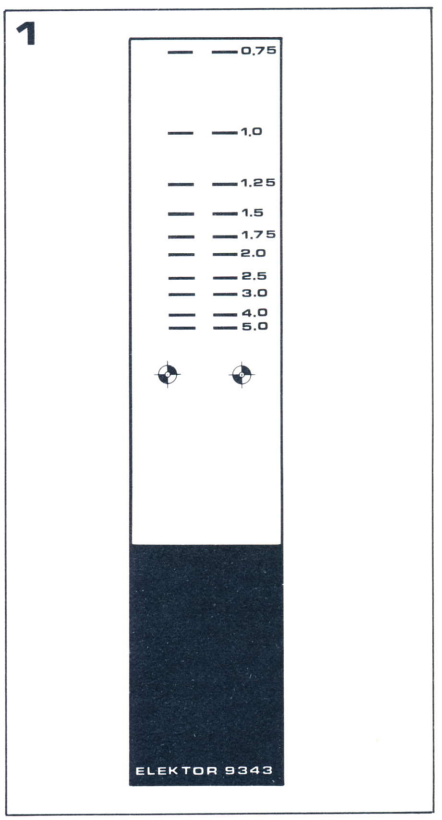
Correct setting of stylus tracking force is of utmost importance – certainly for modern 'feather-weight' cartridges. The gauge that is built in to many modern record players is not always reliable, so a double-check by means of a separate balance is often advisable.



The 'ideal' tracking force for most modern cartridges is somewhere in the 0.75 . . . 3 gram range.
Most manufacturers specify the minimum and maximum permissable tracking force for their cartridges. In practice, the best value usually proves to be just under the specified maximum. It is perhaps worthy of note that the danger of damage to the record is greater if the tracking force is too low than if it is too high – within moderation, of course! As a rule of thumb, the maximum for dynamic cartridges with an elliptical stylus is about 1.5 g, whereas the maximum with a spherical stylus will be about 3 g. From the above it will be obvious that a useful measuring range for a stylus balance would be 0.75 . . . 4 grams.

The p.s.b.

The simplest type of measuring instrument for tracking force is a balance – and it can also be one of the most accurate types.
An easy way of making such a balance is to use epoxy printed circuit board material. Computer aided design has resulted in the end product shown in figure 1: the printed stylus balance or p.s.b.
Round-headed furniture tacks, rivets or the like can be used as pivots. These are pushed through the holes until the heads lie flush against the back of the board. Due care should be taken at this stage: the calibration accuracy depends on the position of the pivots, and any sharp edges (such as deep scratches) can affect the freedom of movement.
The calibration depends on the mass per unit area of the material, of course; the scale shown is accurate for the boards supplied by the Elektor p.c. board service (EPS 9343).

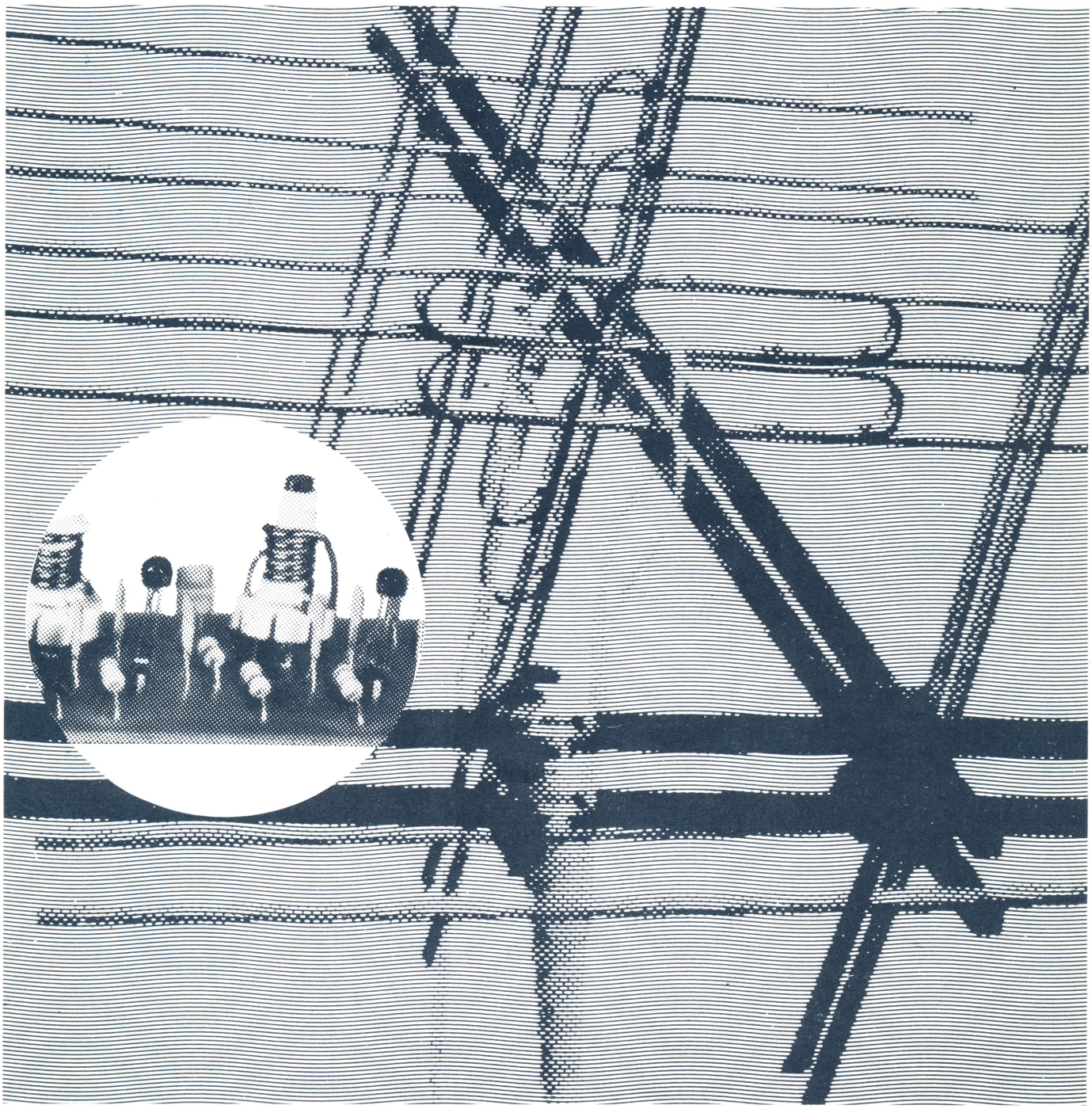


How to use it

The balance is placed on the turntable so that it pivots on the round heads of the tacks (see photo). The stylus is now gently lowered onto the balance, and by sliding it up or down along the open track between the calibration marks (rotate the turntable a fraction) the position can be found where the whole set-up is in equilibrium. The tracking force can now be read off.
For the highest degree of accuracy it is advisable to set the anti-skating compensation at '0', and to level the record-player. The latter is always a good idea, anyway, in the interest of minimum wow.

tunable aerial amplifier

The aerial amplifier described in this article is characterized, among other things, by its low noise level (1-2 dB), a voltage gain of 10-20 dB, and a wide tuning range (146-76 MHz).
It is designed for use as an FM-aerial amplifier, although it is relatively simple to modify it for application as a TV aerial amplifier.



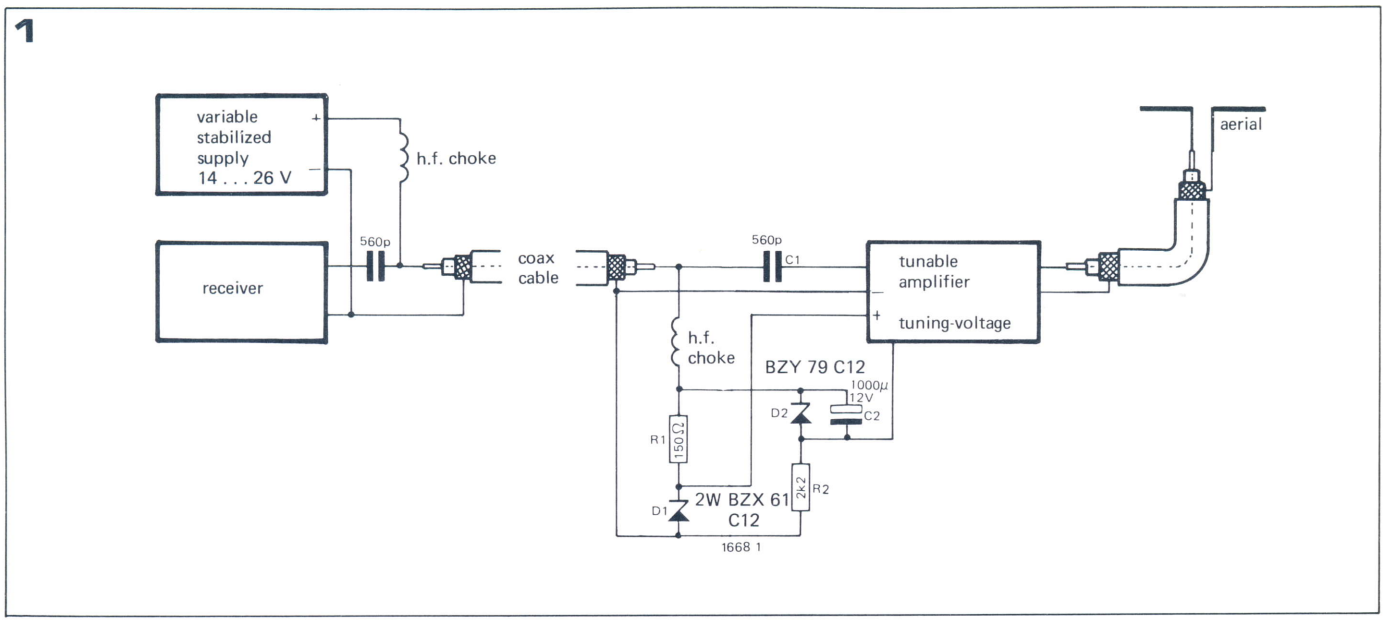


Figure 1. With simple means the coax cable can be used for the signal-, the supply- and the tuning voltages.

Aerial amplifiers can be divided roughly into two categories: wideband and tuned. The main advantage of wideband types is, of course, to be found in the fact that a frequency spectrum of several decades can be amplified without anything having to be switched over or readjusted. On the other hand, there are some drawbacks that count all the more if the amplifier is expected to provide maximum improvement in reception quality.

Using wideband amplifiers entails the following drawbacks:

1. Cross modulation soon occurs because the total amplitude offered can be fairly large. Furthermore, the entire amplified spectrum is fed to the receiver and this is another likely cause of cross modulation.
2. In most cases it is impossible to design a wideband amplifier for minimum noise contribution. This is because the cable impedance (usually 60 Ω) is not the optimum value for the amplifier. In addition, it is almost impossible to compensate fully for parasitic capacitances.

Comparison of the noise contributions of TV tuners and of wideband amplifiers shows that both are usually of the same order of magnitude for the UHF band. In the VHF-TV and the FM bands, the tuner often has an even lower noise figure than the wideband amplifier. If the wideband amplifier gives better reception, this is due mainly to the fact that when the amplifier is placed between the aerial and the cable, the cable losses become far less important.

Tunable amplifier

A drawback of a tunable amplifier is that an extra cable is usually needed for the tuning voltage. By means of a simple circuit, however, (figure 1) it is possible to use a tunable amplifier without an extra cable. The stabilized power supply provides the sum of the supply voltage and the tuning voltage, and within the amplifier the 12 V supply is obtained by stabilization with a voltage regulator diode.

By connecting a 12 V regulator diode in series with the supply voltage, the tuning voltage is 12 V lower than the supply voltage. If the variable stabilized supply is now adjusted from 14 to 26 V, the supply voltage for the amplifier remains 12 V, and a tuning voltage of 2 to 14 V becomes available.

It goes without saying that the variable supply must have a very low hum and noise level to avoid amplitude and phase modulation via the varicaps. Therefore a large electrolytic capacitor is placed in parallel with D2.

The circuit consumes about 100 mA, but offers the advantage that the amplifier always is at a higher temperature than ambient, so that water condensation and the resulting corrosion are avoided.

Design possibilities for tunable amplifiers

A FET-amplifier can be based on two main circuits, to wit: the common-gate and the common-source amplifiers. Since the amplifier is tuned, the input and output capacitances of the semiconductors usually present no problems. Not so, however, the feedback capacitance, because this may give rise to instability. Another important quantity is the input impedance. If we tabulate the necessary design data, we get something like table 1.

Table 1.	common source	common gate
input impedances	specified by the manufacturer; can be anything between 1 and 20 k at 100 MHz	usually deviates no more than 20% from 1/S
output impedance	specified by the manufacturer and is usually of the same order as the input impedance at common source	
feedback capacitance	1-10 p	very low; usually 0.1-0.01 p

The drawback of the common-gate amplifier is that its maximum gain is less than that of the common-source circuit. On the other hand, however, the common-gate amplifier has greater reliability and stability. A secondary advantage is that the difference in matching for minimum noise or maximum gain is much less than for the common-source circuit, and is in some cases even negligible. Radio reception requires matching to minimum noise, TV reception requires matching to maximum power gain to eliminate cable reflection (picture 'ghosts').

The circuit (figure 2)

To obtain a wide matching range, the circuit is designed around discrete coils. This also offers greater freedom as regards using other types of FET. Often mistakes are made as regards the quality factor of such home-made coils; in this case a Q-factor of 100 or more can easily be achieved.

Although the diagram shows the amplifier with asymmetrical input and output, it can easily be adapted for application with symmetrical aerials by providing L1 and L3 with coupling windings. To eliminate the problem of the (wide) tolerance in the pinch-off voltage, the gates are connected to a positive voltage so that each of the FETs draws about 10 mA. For a 12 V supply voltage, the gate-drain voltage is about 6 V, and for most types of FET

this produces the minimum noise contribution. The only limitation to using certain FETs is the slope, which should be greater than 4 mA/V. A larger number of types meet this requirement, as shown in table 2.

Table 2.

type	minimum slope mA/V	db noise contribution (typ) at 100 MHz
E300	4,5	1.5
E310	10	1.5
U1994E	4,5	1.5
2N4416	4	1.2
2N5397	6	1.8
U310	10	1.5
E304	4,5	1.7
SD201 (mos)	13	1.5

The fact that the circuits possess a high-Q-factor does not necessarily imply that the amplifier is a narrow-band type. The circuits are damped by the input and output impedances of the FETs. Suppose the no-load Q-factor is 100. The resonance impedance then found at 100 MHz is:

$$Z = Q\omega L = 15 \text{ k}.$$

The efficiency of a circuit is given by:

$$\eta = \frac{Q_O - Q_L}{Q_O}$$

where Q_O and Q_L represent the quality factor under no-load and load conditions, respectively.
So for a high efficiency it is necessary to load the circuit heavily, which also reduces the effect of the FET output impedance. For the case where $Q_O = \infty$, and the output impedance of the FETs is ∞, the gain is given by (figure 3):

$$A_V = n_2/n_1 \cdot S_1 \cdot (n_3/n_4)^2 \cdot \cdot n_4/n_3 \cdot (n_5/n_6)^2 \cdot \cdot n_6/n_5 \cdot Z_C =$$

$$= \frac{n_2 \cdot n_3 \cdot n_5}{n_1 \cdot n_4 \cdot n_6} \cdot S_1 \cdot Z_C \qquad (1)$$

If we take

$$Z_C = 50 \quad n_2/n_1 = 1.2$$
$$n_3/n_4 = 2.5 \quad n_5/n_6 = 5$$

(1) becomes:

$$A_V = 750 S_1 \qquad (2)$$

From the above formulae it appears that the gain is directly proportional to the slope of the first stage. This is only true, if the ideal condition ($Q_O = \infty$ and infinitely high output impedances) is sufficiently approached, and that is the case here if S2 is at least 4 mA/V.
It is logical, therefore, to use for T2 a cheap FET that meets this requirement, such as the U 1994 E or the E 300. Measurements where T1 = T2 = E 300 indeed showed a voltage gain of 3. When a type E 310 was used for T1 (S = 10 mA/V), the gain increased to about 8.
To investigate the effect of T2 on the gain, first a type E 310 was used, with the result that the gain increased to 10. Since the primary function of an aerial amplifier is to improve the signal-to-noise ratio at the amplifier input, it is pointless to measure the bandwidth at the 3 dB points. It is better to quote the bandwidth in which the noise contribution may deteriorate a certain

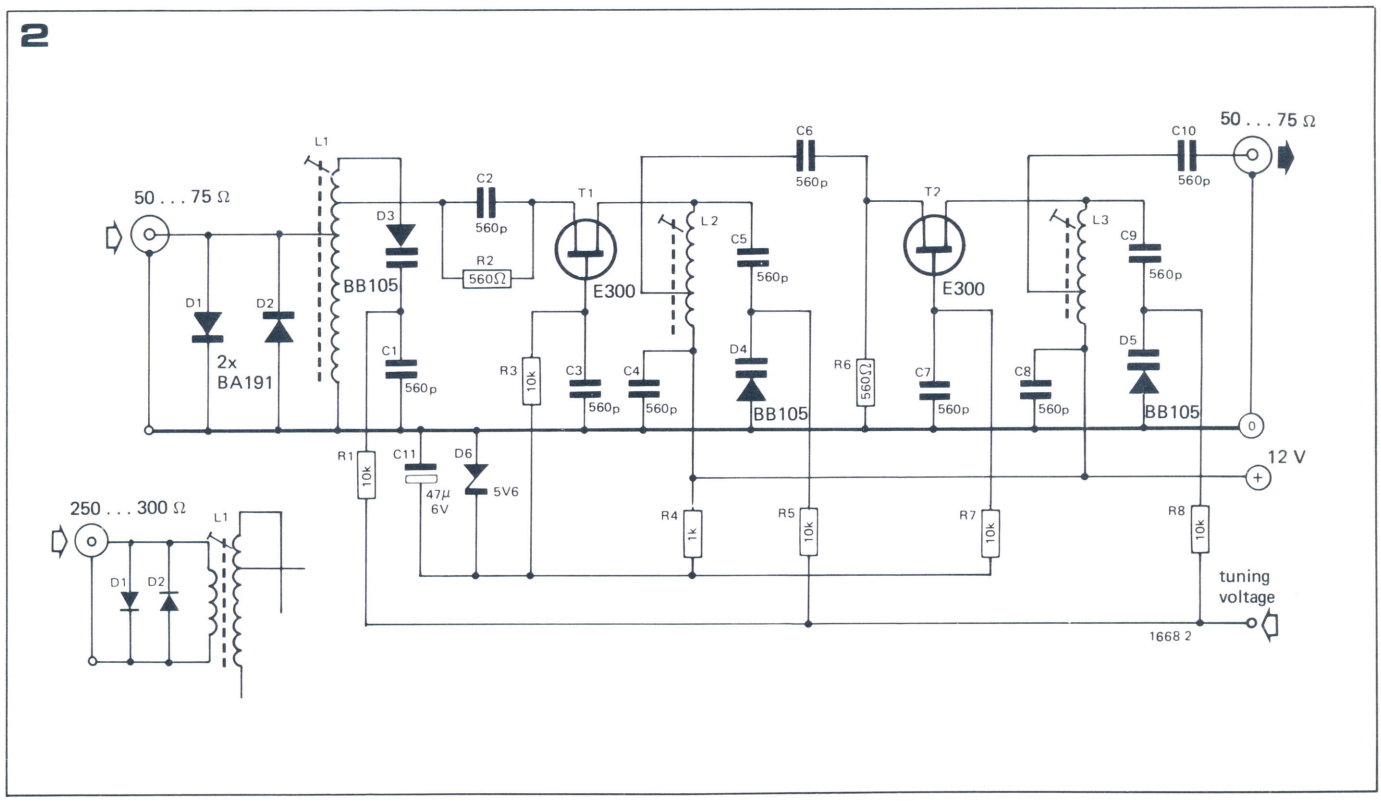
Note:
The FETs mentioned here are supplied by the following manufacturers:
Siliconix : E300, E310, U310, E304;
Teledyne : U1994E, 2N4416, 2N5397;
Signetics : SD201.

Figure 2. Although the supply voltage in the diagram is 13 V, the amplifier can be connected to any supply voltage between 10 and 20 V. At about 13 V the noise contribution is lowest.

Figure 3. This simplified diagram serves for a rough calculation of the gain.

Figure 4. The drawing shows how the coils should be wound.

Figure 5. The method for coil mounting shown here saves considerable time. Overall performance does not suffer, but the appearance is not so neat.



amount, say 0.5 or 1 dB. If this standard is used, the bandwidth of the amplifier is about 3 MHz at 100 MHz, but this could not be measured exactly because the elektor laboratories are not equipped with the (extremely) expensive equipment needed to take accurate noise measurements.

The ratio n_2/n_1 given in the example above, and which is lower than might be expected, was determined empirically for a minimum noise contribution, and this adaption proved to be the most favourable one for both the E 300 and E 310. If the coils are made of silver-plated copper wire, it is quite a simple matter to determine the best tap.

Mounting, construction and adjustment

An important requirement is that all connections must be as short as possible. Photograph 1 gives a clear picture of the mounting. The FETs should have much shorter connecting leads than shown in the photograph (about 6 mm); long leads have distinctly unfavourable effects on stability and the signal-to-noise ratio; this was being verified when this photograph was taken.

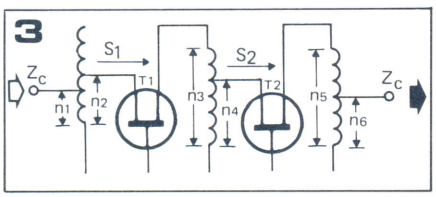
All capacitors, except for C11, are of the low-loss ceramic disc type. Current types of Schottky diodes can be used for D1 and D2, and types BB105A, BB105B and BB105G are suitable for D3 to D5. The coils are wound on Kaschke coil formers type KH 5/22, 7-560-8A, with a ferrite core, type K 3/12/100. Several other types of coil formers might be suitable as well, if the diameter is about ¼ in (6 mm). The ferrite core has to be a VHF-type! The winding data are given in table 3.

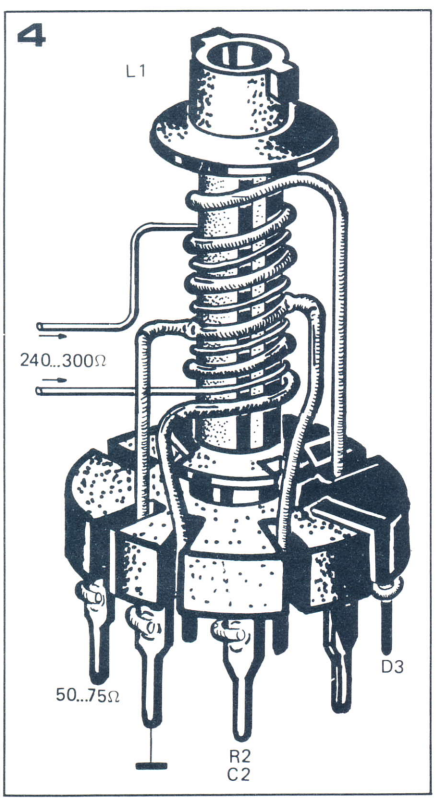
coil	tap with respect to + or $-V_b$	total number of turns
L1	aerial 50/75Ω2	
	240/300Ω4 (coupling winding)	5
	source 2.5	
L2	source 2	5
L3	output 50/75Ω1	
	240/300Ω2 (coupling coil)	5

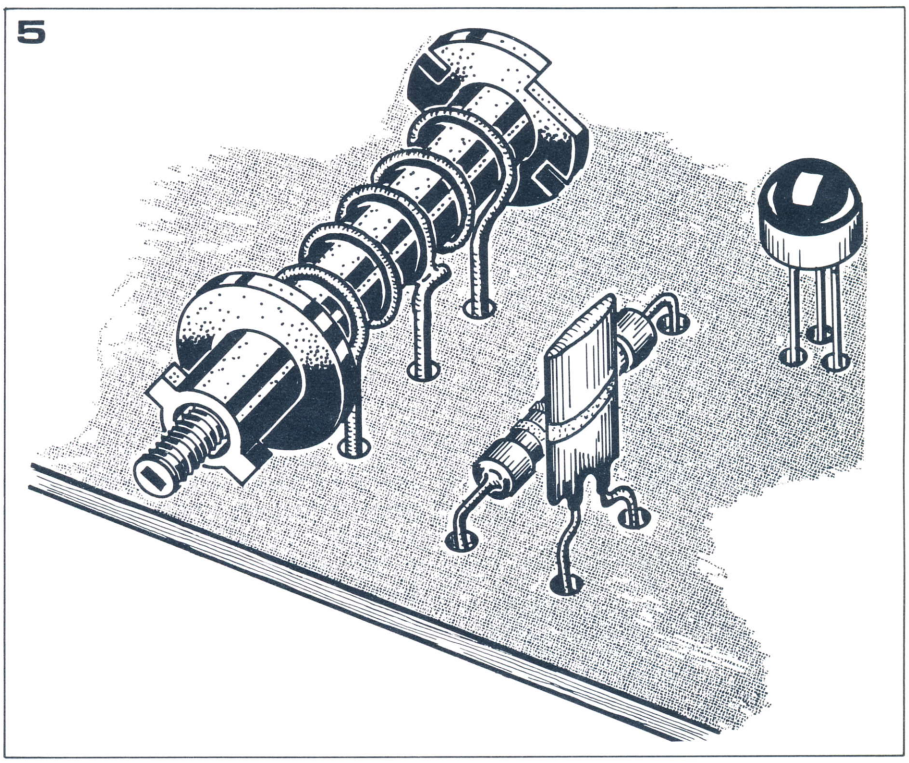
The wire should preferably be silver-plated copper wire with a diameter of 1.2 mm. The spacing between the turns is 0.8 mm and is obtained simply by winding a so-called 'blind wire' of a diameter equal to the spacing, i.e. 0.8 mm, together with the coil wire.

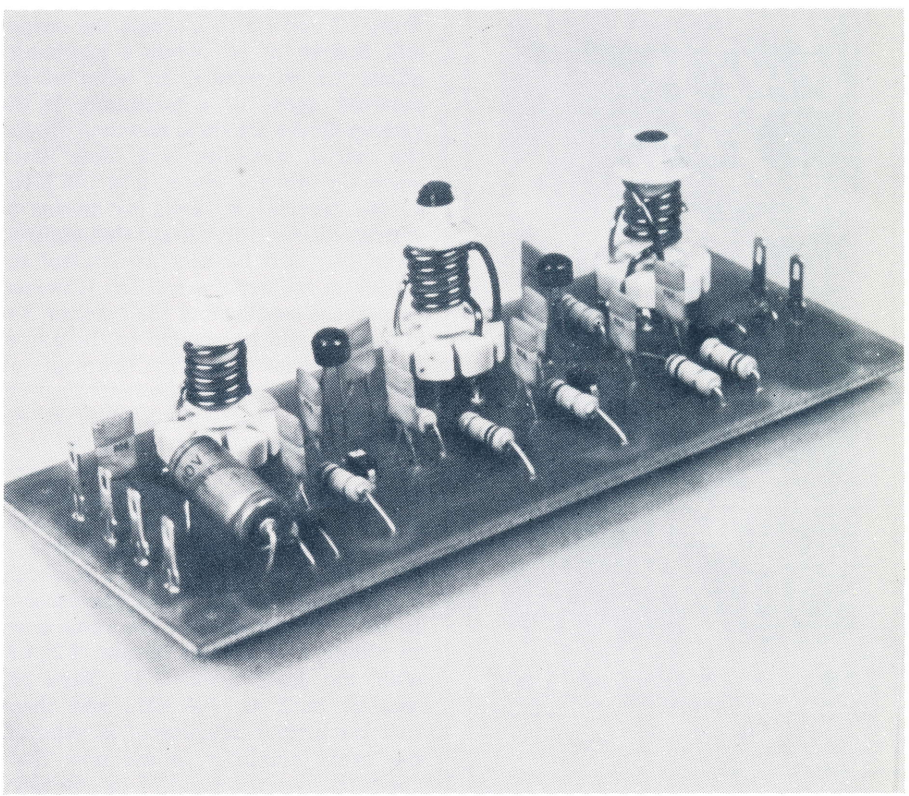
Once the coil has been mounted, this blind wire is, of course, removed unless the 240/300 Ω connections are to be used. In that case the blind wire is 0.8 mm enamelled copper wire, and after mounting of the coil, this blind wire is wound off again until the above number of turns is left.

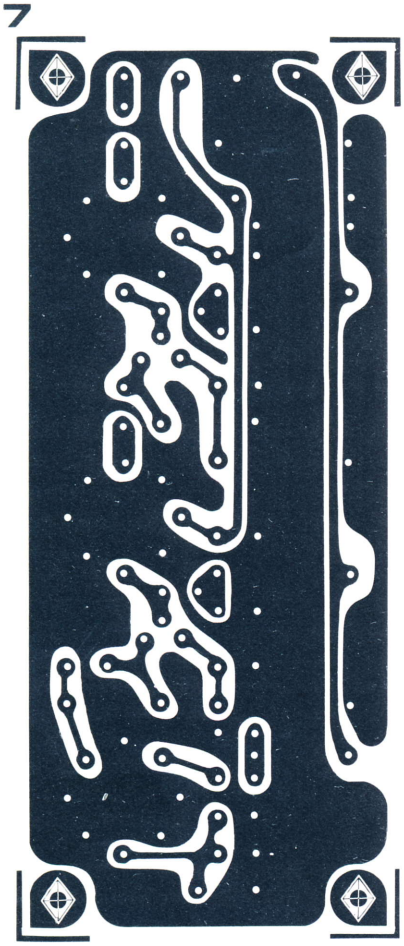
As the coupling coils must be placed at











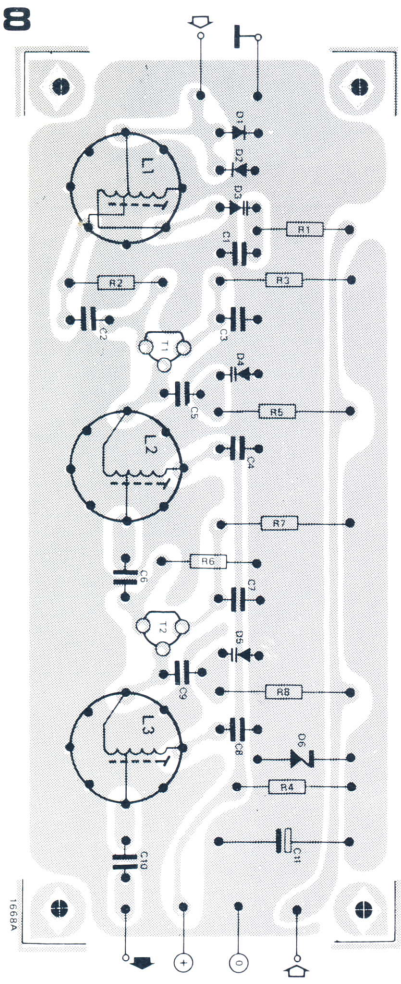


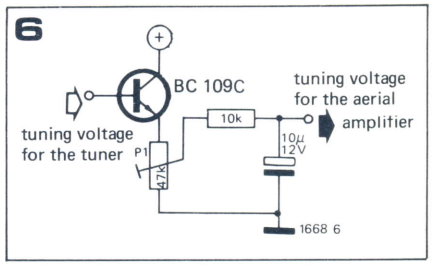
Figure 6. To obtain the tuning voltage for the amplifier from a tuner with a high-impedance tuning voltage, such as tap presets for instance, an emitter follower is required. If a low-impedance tuner voltage is used, the tuning voltage for the amplifier can be obtained directly via the 47 k adjustment potentiometer.

Figure 7. Layout of the printed circuit board. (EPS 1668).

Figure 8. Component layout on the PC board in figure 7.

the 'cold end', winding back takes place from the coil end that is connected to the varicap. This is illustrated in figure 4. Soldering the wires to the former pins is a time consuming job, particularly for the wire diameter quoted here. If more value is set upon efficient mounting than on appearances, the coils are mounted directly in the circuit, as shown in figure 5. The coil formers will fit only after clipping, as can be seen in this figure. In this case the coils are wound on a drill with a slightly smaller diameter (about 0.1 mm) than the outer diameter of the coil former.

If the receiver used is not tuned by means of varicap diodes, the aerial amplifier should be adjusted as follows. Set the ferrite cores half way in the formers. Tune the receiver to a weak station with a frequency of about 95 MHz and adjust the tuning voltage – the voltage applied to the varicap diodes – to obtain a maximum output. Tune L2 and L3 to increase the output still further or to obtain a maximum; adjust L1 to reduce the noise of the received signal to a minimum. If the varicap diodes are three matched diodes, the aerial amplifier will now track correctly over the range 76 to 146 MHz. If the receiver is tuned by means of varicap diodes, the voltage that controls them can also be used to control the diodes in the aerial amplifier. However, to prevent overloading the receiver, the voltage should be applied to the diodes in the aerial amplifier through an emitter follower as shown in figure 6. The tuning procedure now is as described above, except that a weak station with a frequency of about 88 MHz should be used and P1 is set to give a maximum tuning voltage. Next turn the receiver to a weak station at 100 MHz, and again adjust P1 to obtain a maximum output. Tune the receiver to 88 MHz and readjust the three cores to obtain a maximum output (L2, L3) with the least noise (L1). Tune the receiver back to 100 MHz and check that no further adjustment is required; the aerial amplifier should now track correctly over the band 76 to 146 MHz.



Parts list

resistors:
R1,R3,R5,R7,R8 = 10 k
R2,R6 = 560 Ω
R4 = 1 k

capacitors:
C1 . . . C10 = 560 p ceramic disc.
C11 = 47 µ, 6 V

semiconductors:
D6 = 5V6 regulator diode

other semiconductors: see text!

If further adjustment is needed, then repeat the whole procedure until it is not.

Results and application in the 2 m amateur band

The sensitivity of FM tuners can be limited by:

1. the signal-to-noise ratio at the input, and
2. insufficient amplification of the intermediate frequency.

Most factory-made receivers are designed so that a combination of these two factors is operative. Although it is difficult to give an exact rule for the improvement obtained by using the amplifier, it may be expected that the sensitivity of the receiver will improve by about a factor of 3 for the same signal-to-noise ratio. If still greater amplification is required, the amplifiers can be cascaded. An amplification factor of more than 10, however, will usually give rise to cross modulation in the receiver; the same amplification can also be obtained by means of one amplifier equipped with FETs that have a steep slope. The coils described can be used in the two-meter band, but the varicaps must then be replaced by ceramic trimmers of 1-9 pF. The bandwidth is more than sufficient to cover the entire band.

Conclusions

The aerial amplifier discussed in this article is suitable for many applications and has such a low noise figure that it will improve reception in all cases. Apart from the 76-146 MHz range, the amplifier, with modified coils, can also be used to great advantage in the following bands:

14, 21 and 28 MHz amateur band, channel 2-4 TV, channel 5-12 TV, and perhaps the UHF band.

miniature amplifier

For the younger constructor with limited funds it is necessary to be very cost-conscious when designing circuits. This circuit for a simple record player amplifier fulfils these requirements. The circuit will operate from a 4.5 V battery and can be used to amplify the output of a crystal pickup to drive a small loudspeaker or headphones. The circuit is not outstanding for its power or quality, but it is simple and reliable.

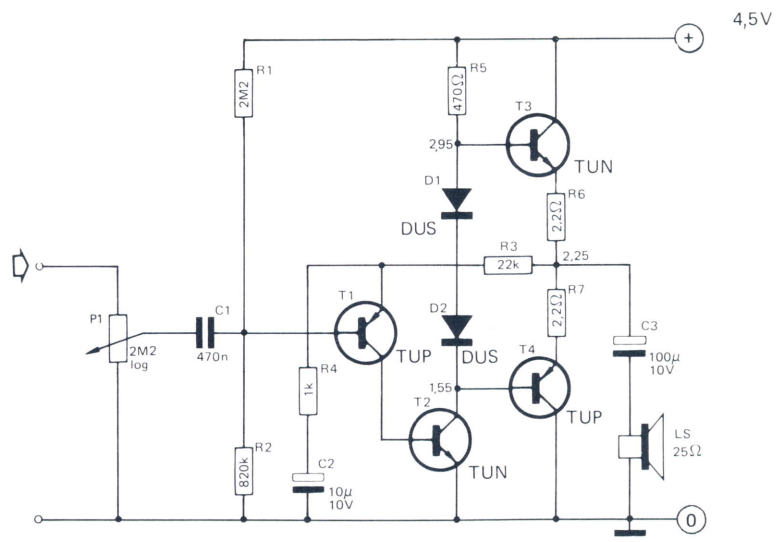
The input and driver stages T1 and T2 operate as voltage amplifiers. The output stage, T3 and T4, operates in class B to achieve long battery life. D.C. feedback is provided by means of R3 and A.C. feedback by means of R3, R4 and C2. This defines the gain, stabilises the operating point and increases the input impedance.

The biassing of T1 is critical and the values for R1 and R2 must be adhered to. Should the circuit fail to operate correctly the D.C. conditions may be checked at the base of T3 and T4 and the junction of R6 and R7.

If 25 ohm loudspeakers are difficult to obtain, then 8 or 15 ohm types may be used instead. In that case R6 and R7 should be replaced by wire links.

As can be seen from figure 2 the p.c. board is extremely miniature and finding space in the record player cabinet should be no problem. To improve loudspeaker efficiency the loudspeaker cabinet should be as large as possible.

1



Input impedance $Z_1 \geqslant 600$ k
Input sensitivity v_i = 200 mV (r.m.s.)
Output power (with 25 Ω) P = 50 mW.

Figure 1. The very simple amplifier circuit.

Figure 2. Layout of match-box size printed-circuit board.

Parts list.

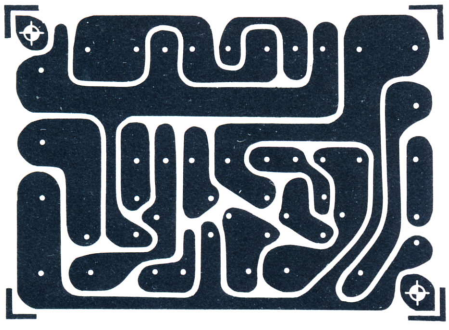
Resistors:
R1 = 2M2
R2 = 820 k
R9 = 22 k
R4 = 1 k
R5 = 470 Ω
R6 = 2.2 Ω
R7 = 2.2 Ω
P1 = 2M2 log

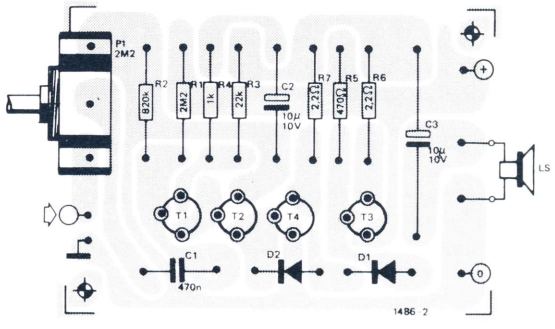
Capacitors:
C1 = 470 n
C2 = 10 µ/10 V
C3 = 100 µ/10 V

Semiconductors:
T1,T4 = TUP
T2,T3 = TUN
D1,D2 = DUS

Sundries:
Torch battery 4.5 V
Loudspeaker 25 Ω

2





mos clock 5314

The 'brain' in the digital clock described in this article is the clock-IC MM5314, which needs only a few external components. The time of day is indicated by seven-segment Ga-As displays, which are now offered at quite agreeable prices. Another attractive feature is that if no seconds reading is included in the design, a considerable saving can be made, whilst seconds indication can always be added at a later stage.

The clock-IC

The clock integrated circuit type MM5314 is designed to indicate the time in hours, minutes and seconds with the aid of seven-segment displays. In contrast to the MM5313 it has no BCD output. Consequently, it is smaller (DIL 24 pins), has a simpler construction, and, what is perhaps even more important, is a lot cheaper. However, as appears from the circuit diagram of the MM5314 (figure 1), all the components needed for building a clock are available.

The IC receives its clock pulse from the mains, and can be used for 50 Hz or 60 Hz drive. The supply voltage may vary from 8 V to 17 V and need not be stabilized. If not connected, all drive inputs are at '1' level because resistors are incorporated which connect them to the plus pole of the supply voltage.

As regards the clock design, the IC offers the choice of various possibilities that depend only on a certain logic state of the drive input concerned.

It is possible, for instance, to choose between a 24-hour and a 12-hour cycle. With the 12-hour cycle the leading zero indication is automatically suppressed, which saves a lot of power. If in addition no seconds reading is required, two seven-segment displays and two transistors can be omitted, which gives a considerable saving. By means of the input 'strobe', read-out can be suppressed, and there are, of course, control inputs for retarding or advancing the clock. The clock can also be stopped for correct time setting. The table gives all possible settings of the control inputs. Figure 2a shows a top view of the pins of the MM5314 integrated circuit.

Operation

In the overall circuit of the IC two main sections can be distinguished:

a. the counter with corresponding circuits
b. the circuits for decoding and driving the displays (surrounded by the dashed line in figure 1).

Pulses to drive the counter are obtained from half cycles of the mains supply. The pulse shaper at the input of the counter changes the sine-waves into square waves by means of a Schmitt trigger. This trigger has a hysteresis of about 5 V. Depending on the logic state at pin 11 of the IC, the pulse signal is divided by 50 or 60, so that a signal of 1 Hz becomes available for the next divider. In the next three stages of the counter the pulse signal is divided into minutes and 12 or 24 hours, depending on the cycle chosen, and determined by the logic state of pin 10.

Via the gates of the individual stages of the counter the clock can be set correctly. If pin 14 of the IC is at '0', the clock will run at the rate of 1 minute per second. If pin 15 is at '0', the hours will run at the rate of 1 hour per second. When pin 13 is at '0', the clock is stopped. If a 12-hour cycle is chosen, the leading zero is suppressed by a special circuit in the IC.

Counter read-out and display drive are achieved with a multiplex technique. The multiplexer senses the various counter positions successively in the rhythm of a multiplex frequency, and passes the value found to a decoder, and from there to an output memory (ROM-Read Only Memory). The multiplex frequency can be varied by means of a simple RC network connected to pin 23. The multiplex oscillator is followed by a divider that, depending on the logic state of pin 24, produces four- or six-digit drive pulses (with or without seconds, respectively). Using the multiplex technique implies that the displays are not driven in parallel, but in series. Parallel drive means that all counter positions can be read out simultaneously. To that end the counter reading of each decade is, at a certain moment, fed to a memory corresponding to each decade. The information thus stored drives the displays of the counter readings via a decoder. This happens simultaneously for all decades; hence the term parallel drive. Multiplex technique, however, means that all counter readings are scanned quickly in successive order and are fed in the same order to an output memory (ROM), which for this IC is programmed for seven-segment displays. At the same time that the counters are read, each corresponding display receives the supply voltage via the drive logic of the block marked 'Digit Enable'. This means that, with this clock, the counters can be read 1 out of 4 if a four-digit display is used, or 1 out of 6 for a six-digit display; the logic state of pin 24 determines the display mode. If, for instance, the one-second counter is read, the one-second display receives supply voltage via 'Digit Enable', and the reading of this decade becomes visible. Corresponding segments of each display are interconnected, but only the particular segments of a display that receive a voltage will light up. In spite of the fact that series drive is used, visual read-out remains constant, provided the multiplex frequency is higher than about 100 Hz. In the MM5314 the multiplex frequency can be chosen up to 60 kHz. If the read-out is suppressed via pin 1 ('strobe') of the IC, the clock will continue to run normally. Thanks to this feature it is quite easy to build an emergency supply.

The circuit

The complete circuit in figure 3 shows that apart from the MM5314 only few components are needed to build a complete clock, Perhaps somewhat unusually, the circuit description starts with the supply, because it is from there that the counter pulses are derived. Since the supply voltage for the IC need not be stabilized, the source has been kept as simple as possible. The d.c. supply voltage may be anything between 8 V and 17 V.

The half cycles of the 50 Hz mains are fed to the pulse input via a decoupling network R22/C3. This input is protected against overloading by means of diode D1.

The RC network (R23/C4), connected to pin 23 of the IC, determines the

Figure 1. Block diagram of the MM5314 integrated circuit. From this it is clear that the entire clock, except the supply and drive for the displays, is incorporated in this IC.

Figure 2a. The pins of the IC seen from the top.

Figure 2b. Pin details of the Opcoa red GaP seven-segment display type SLA1. With most other types of seven-segment displays separate anodes are also connected to pins 3 and 9; hence, an extra connection is needed between these pins and pin 14.

multiplex frequency which, for the given values, is about 10 kHz, Because the integrated circuit cannot provide sufficient current to drive the seven-segment display simple buffer stages are required. These use normal TUN's and are connected between pins 3 to 9 and the display segments. The collector resistors provide current limiting for the segments, so their values determine the luminous intensity of the displays. The minimum permissible value for these resistors is 330 Ω ($+V_b$ = 17 V), in practice 470 Ω gave satisfactory results for all supply voltages. A lower value produced no noticeable increase in luminous intensity, so that in fact only the life of the display is then unnecessarily shortened.

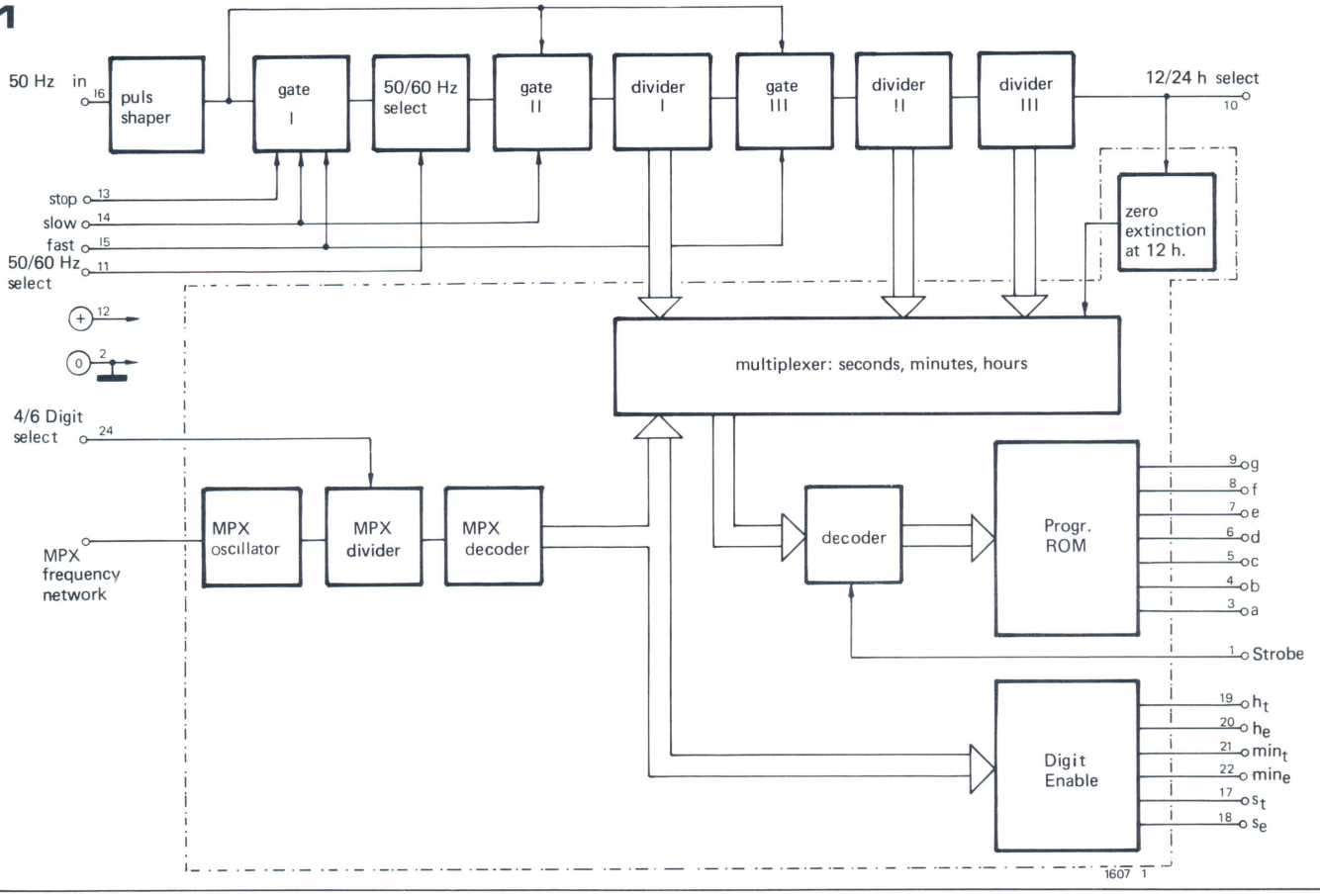
Buffer transistors, acting as switches, are also connected between the 'Digit-Enable' outputs and the anodes of the displays. These switches connect the

Table

function	state*	pin
stop	'0'	13
slow adjustment	'0'	14
quick adjustment	'0'	15
mains frequency 50 Hz	'1'	11
mains frequency 60 Hz	'0'	11
12-hour cycle	'0'	10
24-hour cycle	'1'	10
with seconds	'0'	24
without seconds	'1'	24
strobe	'0'	1

*) An unconnected input is at state '1' because within the IC these inputs are connected to the plus of the supply voltage via resistors.

1



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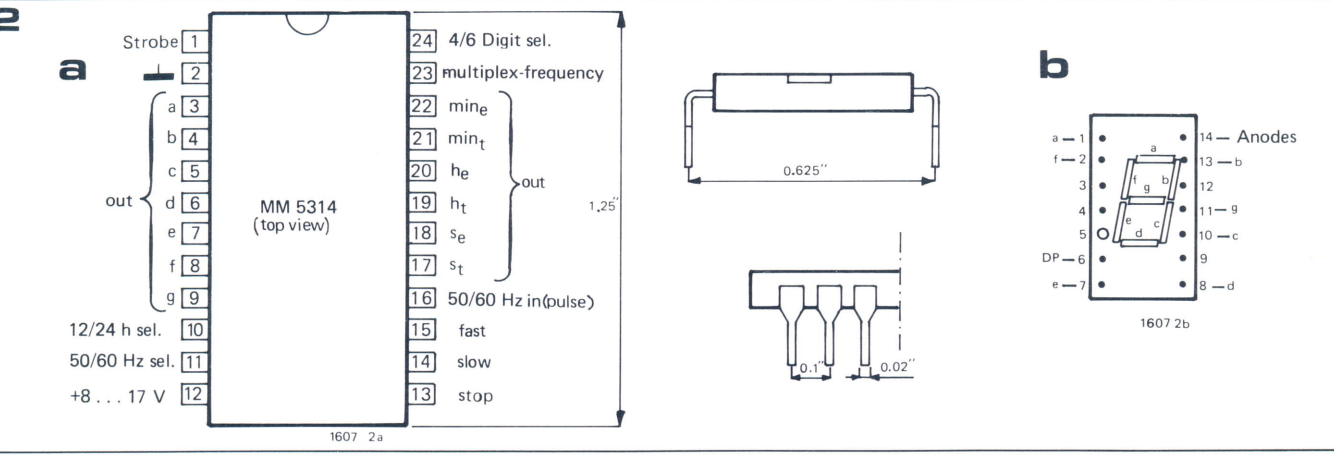
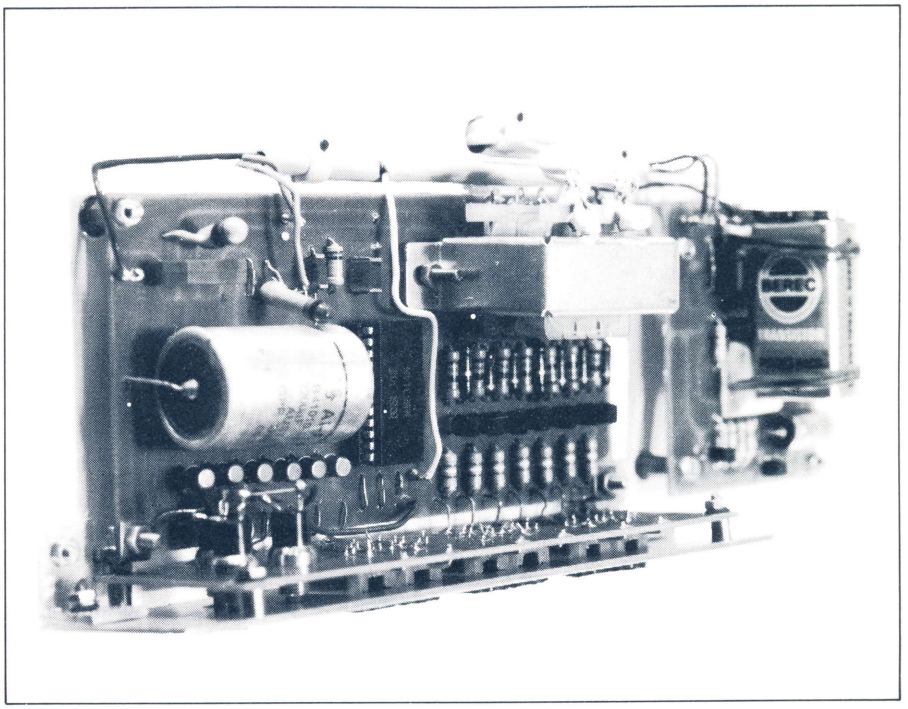


second-, minute- and hour displays to the supply voltage at the correct moment. The switching transistors used here are TUPs.
The circuit is mounted on two printed circuit boards: one for the displays, and one for the actual clock circuit with mains supply.



Printed circuit boards

Figure 4 shows the printed circuit board, and figure 5 the component layout for the mains-fed clock circuit. The boards are quite small, so that the whole unit can be housed in a small attractive cabinet. So much space has been reserved on the board for the supply transformer and electrolytic capacitor C2 that, if necessary, fairly large types can be used. All terminals and controls (50/60 Hz selection, strobe, etc.) are placed in a row on one side of the board, directly opposite the terminals they are connected to on the display board, which is shown in figure 6. This display

3

Parts list

Resistors:
$R_1 \ldots R_7$ = 10 k
$R_8 \ldots R_{14}$ = 100 k
$R_{15} \ldots R_{21}$ = 470 Ω
R_{22}, R_{23} = 100 k

Capacitors:
C_1 = 5n6
R_2 = 2200 µ/25 V
C_3 = 10 n
C_4 = 22 n
C_5 = 47 n

Various:
Tr = mains trafo, 8 . . . 12V/250 mA
$S_1 \ldots S_3$ = miniature push-button, SPST
IC-socket (24 pin DIL)

Semiconductors:
IC = MM5314
$T_1 \ldots T_7$ = TUN
$T_8 \ldots T_{13}$ = TUP
D_1 = DUS
B = bridge rectifier B30C500, BY 164 etc.
Displays = Opcoa SLA 1, Monsanto MAN 1, MAN 7 and MAN 10, Hewlett Packard 5082-7730, Litronix Data Lit 707

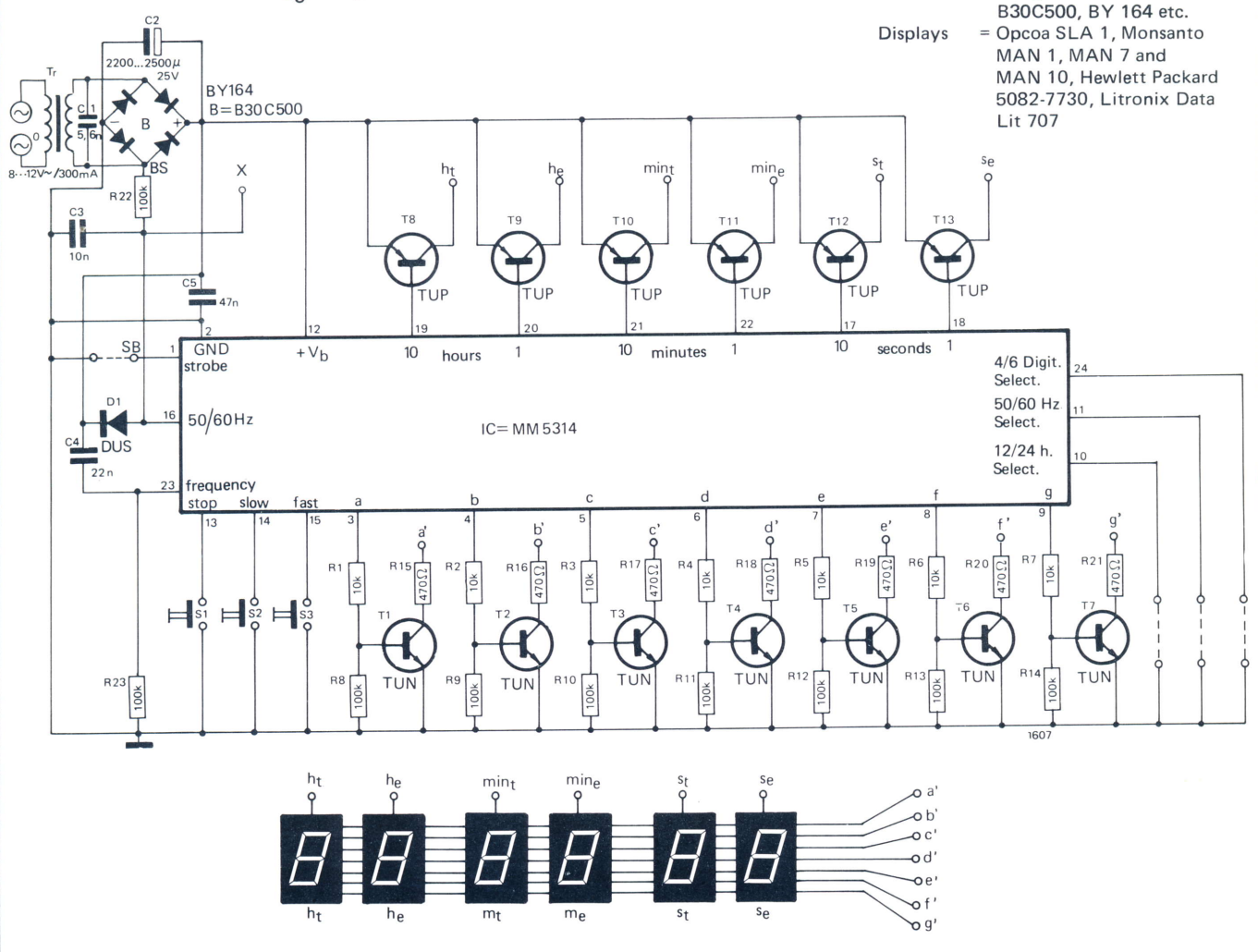


Figure 3. The total circuit complete with mains supply. If instead of TUNs, quality transistors are used for T1...T7 (e.g. BC107), the resistors R8...R14 can be omitted.

Figure 4. The printed circuit board of the clock circuit with mains supply. The pins are positioned so that only very short connections are needed between clock and display circuit boards.

Figure 5. Component lay-out for the clock circuit. There is sufficient space for almost any type of transformer. Even a 40 V electrolytic capacitor could be accommodated on the circuit board.

board holds the displays and small push buttons for 'stop', 'slow' and 'fast'.

Displays

The display board (figure 6) is mounted behind the front plate of the cabinet. Instead of the seven-segment LED displays used here (the Opcoa SLA1), types MAN1, MAN7 and MAN10 of Monsanto, T6302 of Texas, 5082 and 7730 of Hewlett Packard or Data Lit of Litronix can be used. Some of these even have two LEDs per segment, which gives a greater intensity at a slightly lower current consumption. Unfortunately, there are many displays where not all anodes are connected to pin 14, but have separate anodes connected to pins 3 and 9. The pins 3 and 9 (at the bottom of the displays concerned) must then be bent completely inward and connected to pin 14.

With or without seconds

If the 'seconds' indication is not used the expense of two displays, two sockets and two transistors can be saved. In this case there is no connection between pin 24 and earth. Since the board is designed for six displays, two more can always be added at a later time without much trouble.

Connection between the boards

In total (including the seconds) there are 13 control connections between the clock and the display circuit boards. The six pins of Digit Enable (h_t, h_e, m_t, m_e, s_t, s_e) are connected to the corresponding terminals on the display board. Furthermore, the terminals a to g of the clock circuit are connected to the same terminals on the display board. Three other connections run to the three small push-buttons for setting the clock. One side of each button is connected to the supply common.

By means of time signals on the radio, TV, or telephone service, the clock can be started properly and quite accurately. With the buttons 'fast' and 'slow' the clock is pre-set before the time signal

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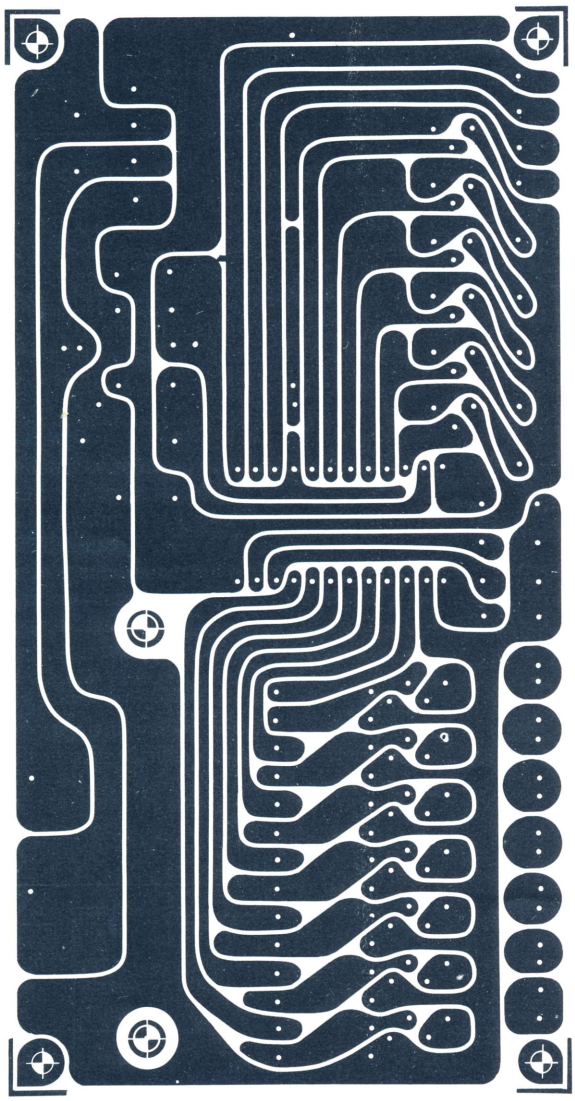

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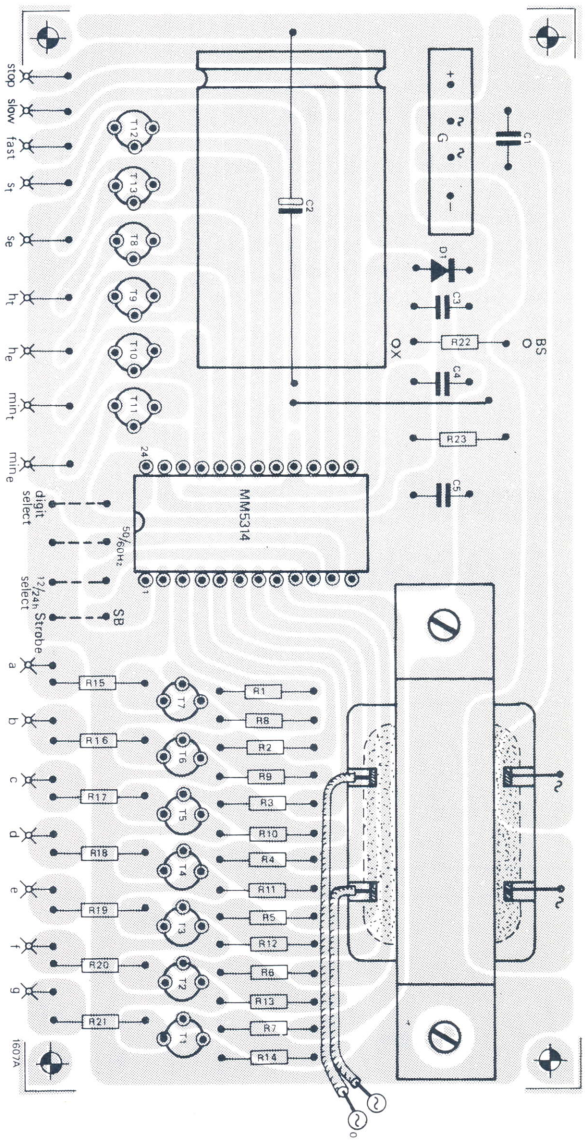
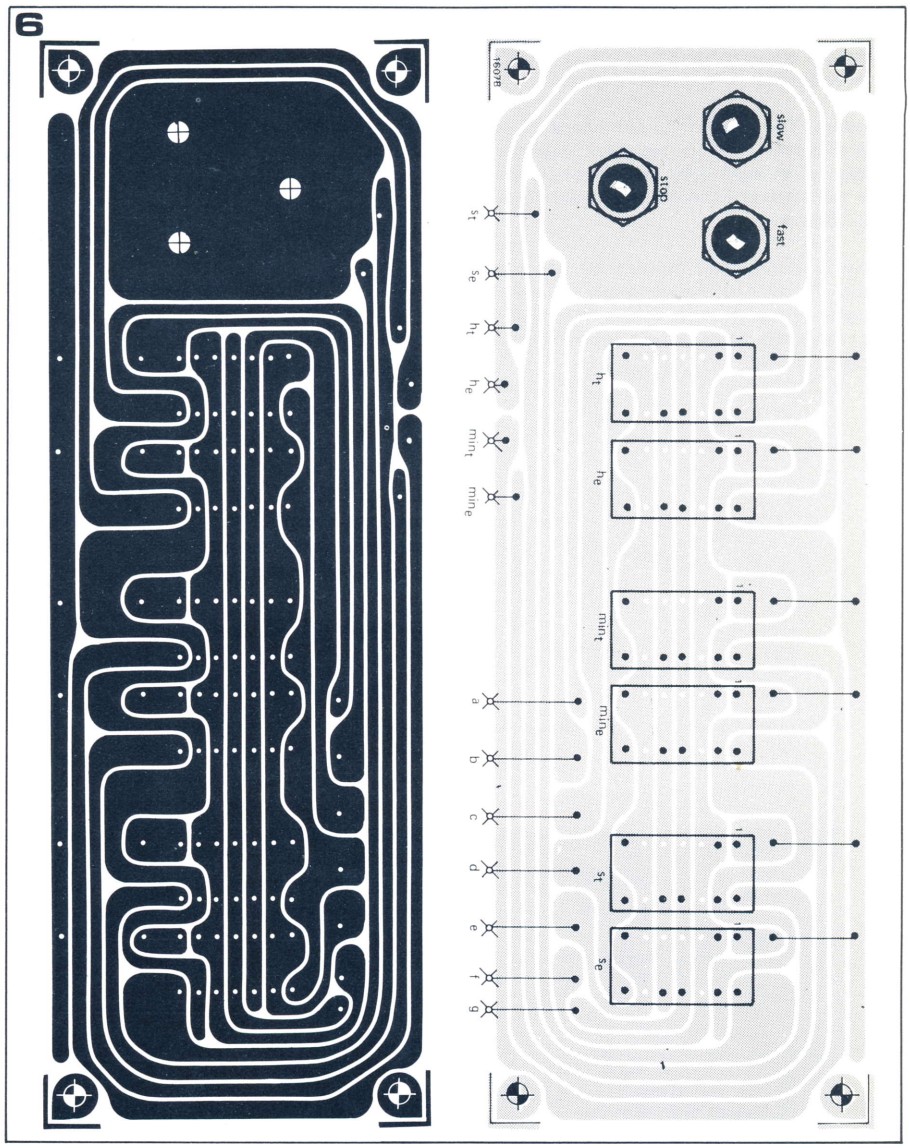


Figure 6. The display circuit board. The small buttons for setting the clock are at the front.



comes, and the button 'stop' is released the moment the signal sounds. The front of the cabinet must have openings for the four or six displays which can be mounted behind perspex, for instance.

Further developments

In Elektor laboratories the following additional units have been developed for the clock:

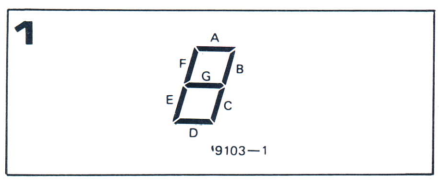
– crystal-controlled time base with only one IC; current consumption complete with oscillator: about 90 μA.
– emergency supply in case the mains supply fails.

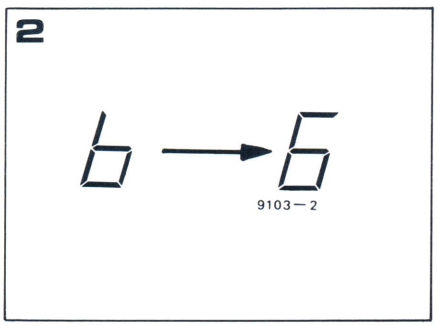
These extensions are discussed elsewhere in this book. The points marked SB, BX and X in figure 3 and in the component lay-out are for use with these units.

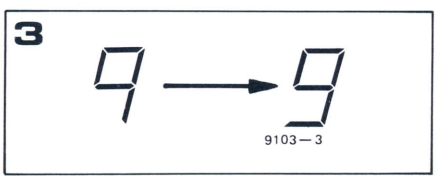
improved 7-segment for MOS-clocks

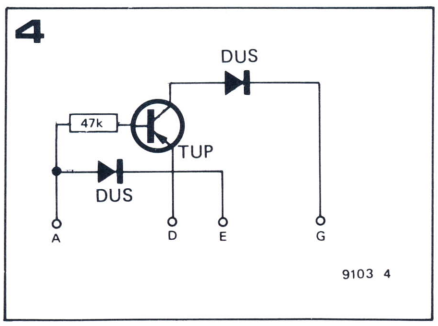
The idea is to add an extra stroke at the top of a six and at the bottom of a nine (Figures 2 and 3).

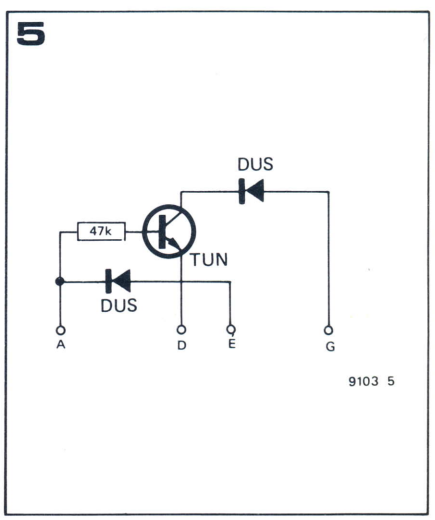
The circuit in figure 4 can be used with common-anode displays, as in the MOS-clock. The points A, D, E and G are connected to the collectors of the corresponding segment-drive transistors (T1, T4, T5 and T7 in the MOS-clock). For common-cathode displays the circuit of figure 5 can be used.



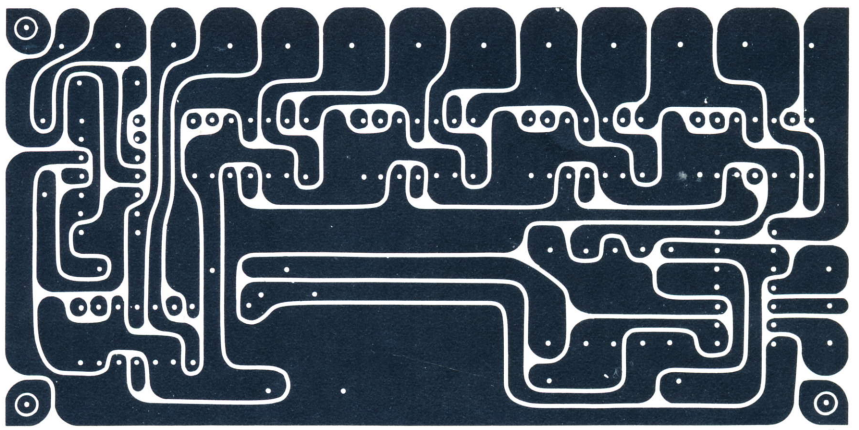


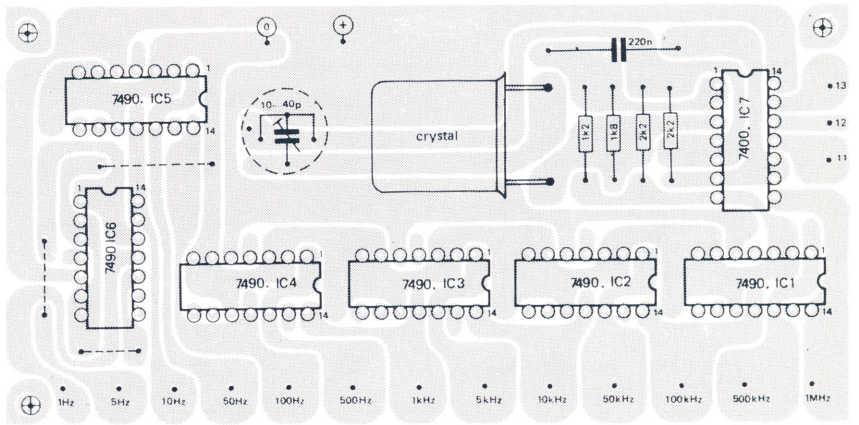


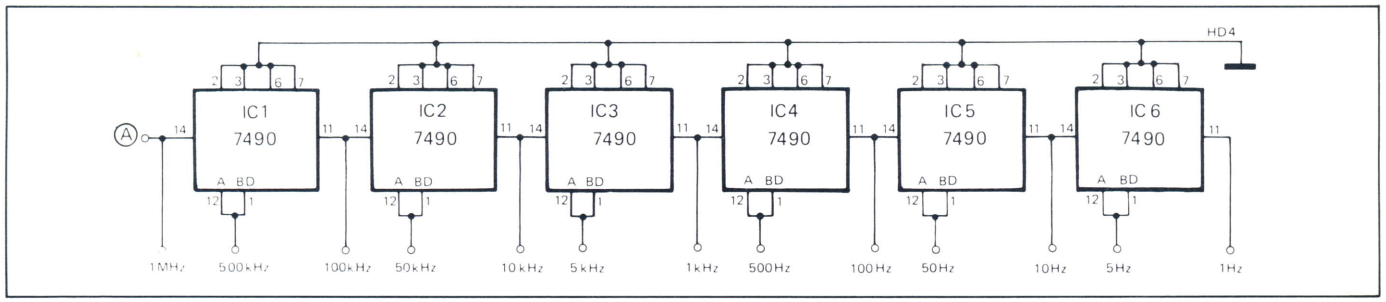




universal frequency reference





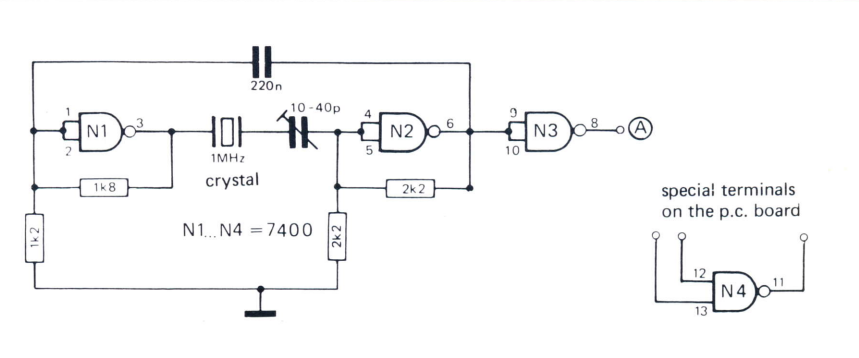


This circuit claims nothing in the way of originality, but is simply a useful, general-purpose board that can be used in many frequency and time measuring applications. It is particularly suitable for use as a gate pulse generator in frequency counters.

The heart of the system is a 1 MHz crystal oscillator based on two NAND-gates. The output of this oscillator is buffered by a third NAND-gate and the frequency is then divided down by a series of 7490 decade counters. These consist of a divide-by-2 stage followed by a divide-by-5 stage, which means that in addition to dividing the reference frequency down to 1 Hz in decades, outputs of 500 kHz down to 5 Hz are also available. These outputs are particularly useful where gate pulses for frequency counters are required. For example, the 5 Hz output will provide positive pulses of 100 ms width, so if the frequency of a 10 MHz signal were being measured a gate pulse this long would let through 1,000,000 cycles of the signal to the counter, giving a display of 1000000. On the other hand, for period measurements the 1 Hz to 1 MHz outputs are more useful. For example, when measuring a one second period, 1,000,000 cycles of the 1 MHz output can be counted, giving a display of 1000000.

The p.c. board layout is quite compact and well laid out. The outputs are available along the lower edge of the board in the diagram. There is one spare NAND-gate in the package used for the oscillator, and this may be used as the gate in frequency counter applications. The connections to it are brought out at the top right corner of the board.

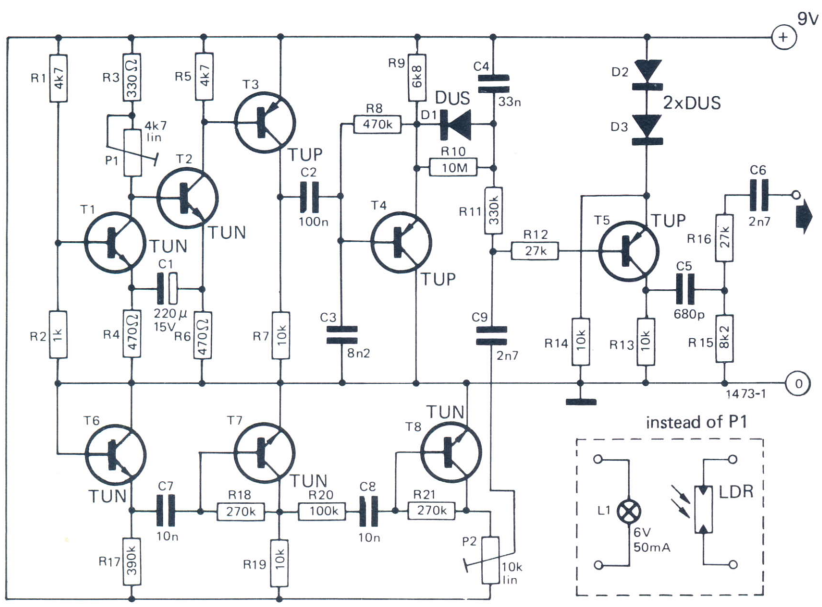
The oscillator frequency may be trimmed to exactly 1 MHz by the trimmer capacitor. The best method of doing this is to use an oscilloscope to compare the 100 kHz output with the 200 kHz Droitwich transmissions, using Lissajous figures. The trimmer should, of course, be adjusted until the Lissajous figure apparently ceases to rotate.



steam train

Many owners of model railways want their 'world of trains' to be as realistic as possible. A means of imitating the sound of a real steam train is, therefore, more than welcome. This article describes a simple method of building an electronic circuit of few components that will produce the required sound. To add even more authenticity, the rhythm of the steam train sound is regulated automatically and is practically proportional to the speed of the train.

1



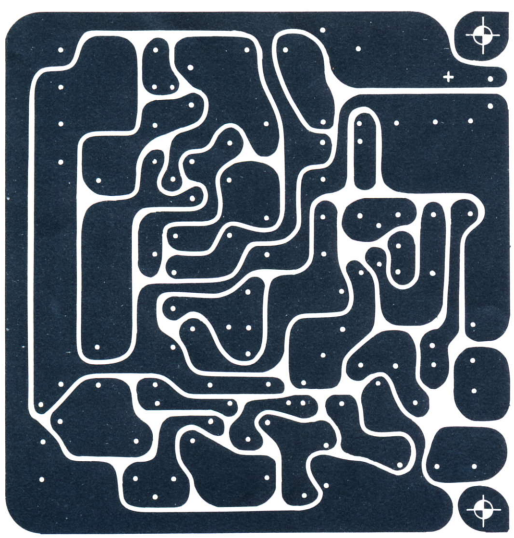
Parts list

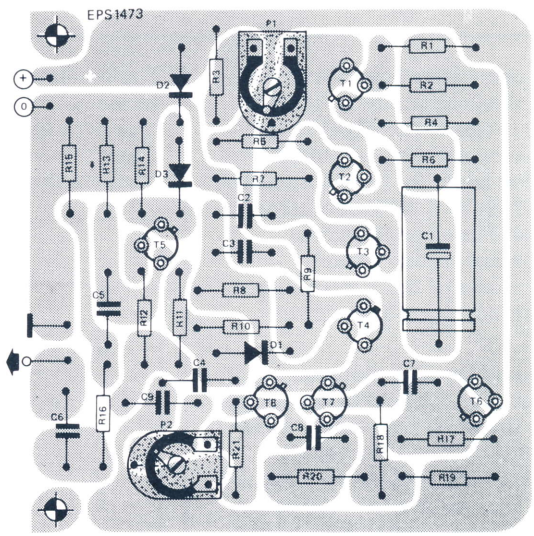
Resistors:
R_1 = 4k7
R_2 = 1 k
R_3 = 330 Ω
R_4 = 470 Ω
R_5 = 4k7
R_6 = 470 Ω
R_7 = 10 k
R_8 = 470 k
R_9 = 6k8
R_{10} = 10 M
R_{11} = 330 k
R_{12} = 27 k
R_{13} = 10 k
R_{14} = 10 k
R_{15} = 8k2
R_{16} = 27 k
R_{17} = 390 k
R_{18} = 270 k
R_{19} = 10 k
R_{20} = 100 k
R_{21} = 270 k
P_1 = 4k7 lin.
P_2 = 10 k, trimmer

Capacitors:
C_1 = 220 µ, 15 V
C_2 = 100 n
C_3 = 8n2
C_4 = 33 n
C_5 = 680 p
C_6 = 2n7
C_7 = 10 n
C_8 = 10 n
C_9 = 2n7

Semiconductors:
T_1,T_2,T_6,T_7,T_8 = TUN
T_3,T_4,T_5 = TUP
D1,D2,D3 = DUS

3





The circuit

Figure 1 shows the complete circuit diagram. The sound of a real engine is produced by the regular escape of waste steam. This hissing sound is produced electronically by a noise generator. The rapid increase and slow fading of the noise as well as its rhythm, is controlled by an astable multivibrator and a pulse shaper. The output of the noise generator T6 is amplified by transistors T7 and T8. The amount of noise, or noise level, can be adjusted by means of potentiometer P2. The transistors T1 and T2 form the astable multivibrator which produces a square wave.

The rhythm of the steam sound can be varied by means of P1. By coupling the spindle of this potentiometer to the speed control on the supply transformer for the locomotive, the rhythm of the steam sound is automatically controlled by the speed of the train. Should this arrangement be too difficult, the potentiometer can be replaced by a light-dependent resistor (LDR); practically any type of LDR will do. A suitable lamp is then connected in parallel with the power supply for the train and placed with the LDR in an opaque envelope to ensure that other light sources, such as room lighting, have no effect.

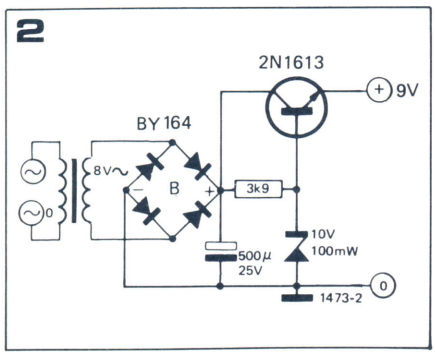
The light intensity now depends on the speed of the train; this controls the value of the LDR and this adjusts the rhythm of the sound to match the speed. To ensure satisfactory control, it may be necessary to try several lamps of different wattage. The capacitors C2, C3 and C4 convert the square wave produced by the astable multivibrator into a certain pulse shape. This pulse drives transistor T5 quickly into conduction, but cuts it off again at a much slower rate. For a short time, transistor T5 then feeds the amplified noise signal to the output while amplifying it even more, after which the amplification is reduced slowly. The output signal can be further amplified by means of an external amplifier or radio set.

The supply

The circuit can be fed from a 9 V battery. Figure 2 shows the circuit for a mains supply.

Figure 1. The electronic steam train circuit.

Figure 2. Circuit diagram for power supply.



steam whistle

Many model railways still run on 'steam'. For greater realism the steam locomotives are nowadays often fitted with an artificial smoke device. They become even more realistic when an imitation steam whistle is also provided.

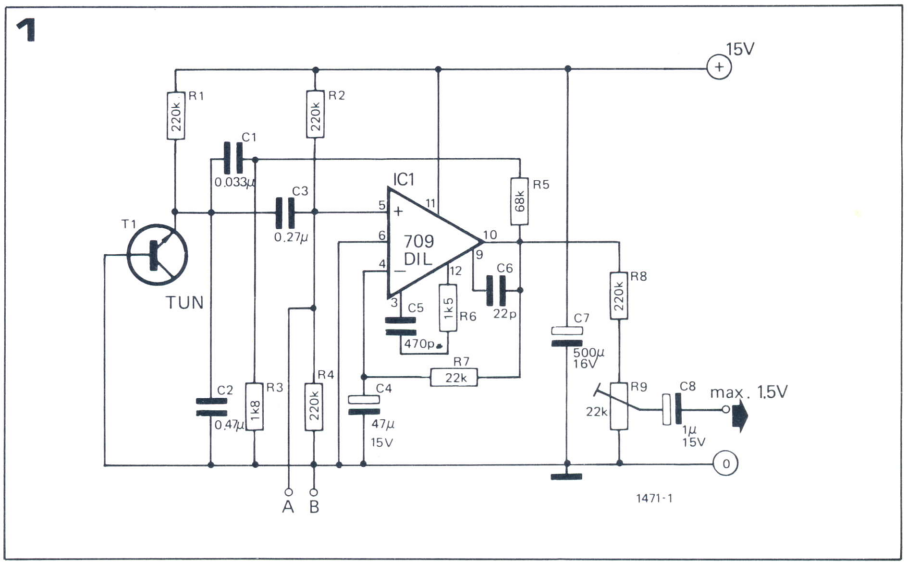


Figure 1. The circuit diagram of the steam whistle. Note the unusual feedback circuit.

In general, electronic imitation of sounds is not so easily done. Analysis of a specific sound by looking at an oscilloscope display, or, better still, with the aid of a spectrum analyser, will make clear just how complicated that sound can be. The spectrum analyser is the clearer, because it displays the various frequency components with their relative amplitudes. But even given sufficient information about the composition of a sound, its electronic imitation is still no pushover. An accurate imitation usually requires a 'truckload' of circuitry.

An acceptable imitation, however, can be achieved with less complication. The problem in this case is nonetheless the same, how to dream up a suitable circuit. Any attempt to seriously calculate component values is futile, particularly when the sound produced is only an approximation to the original. Then there is always the consideration that a spectrum analyser is not normally readily available, never mind a genuine working steam whistle! One is forced to the conclusion that trial and error is the only available approach.

The circuit

We already know two aspects of the circuit. A steam whistle produces a tone, so that the heart of the circuit must be an oscillator. Secondly, a steam whistle is blown – which means hiss. The circuit must therefore also contain a noise generator. This noise generator must modulate the oscillator. Experiment will determine which method of modulation is to be used. Assuming that the brute-force excitation of the original steam whistle gives rise to strong overtones, the oscillator will have to be some kind of multivibrator producing a fairly sharp-edged waveform. The selected square-wave oscillator is a 709 ir a positive feedback arrangement (and including the usual compensation).

The noise-generator is a reverse-biassed base-emitter junction of an NPN transistor.

At the supply voltage of 15 V this junction operates in the breakdown region (Zener), producing plenty of noise. Resistor R1 limits the current to protect T1. Since the noise is directly injected into the oscillator feedback

path, it causes an irregular frequency-modulation of the square-wave. This irregular jittering of the waveform causes the output to sound piercingly shrill – very like a real steam whistle.
The pitch of the note can be varied by changing the values of the capacitors. The influence of the noise generator is largely determined by R3. Varying R3 adjusts the shrillness of the note, but one must bear mind that it will also affect the pitch to some extent.

Keying possibilities

Due to the fact that almost any disturbance of the circuit has an influence on the pitch, it is not possible to key the whistle by electronically switching the feedback. The best approach turned out to be short-circuiting the points A and B. This disturbs the biassing of the 709, causing the oscillation to stop immediately.

This keying can be done, of course, with a push-button (break contact) – but it is much more interesting to let the locomotive switch the whistle on and off.
This can be achieved with a Light Dependent Resistor in two operating modes. The whistle sounds either when light falls upon the LDR or when the LDR is shielded. Figure 2 gives the circuits for both modes. When the whistle is to be started by illumination of the LDR, the circuit with T2 is sufficient. If the triggering is to be done by shadowing the LDR, T3 and R13 have to be added.
The board layout in figure 3 enables either arrangement to be used. In the first case, a jumper lead is required between the base and collector connections for T3.
The positioning of the LDR is very important. When a shadow is to trigger the whistle, the illumination under 'silent' conditions has to be very strong.

A real train usually gives a warning signal just before entering and leaving a tunnel. An LDR positioned under the track will arrange for the model train to automatically do the same. The same applies to a level-crossing. Here once again an LDR mounted under the track, between the sleepers, will greatly add to the realism of a model railway.
Sometimes a quite weak shadow is enough to start the circuit. Some adjustment of the sensitivity is possible with R12.
When the ambient light level in the 'playroom' is on the low side, it will be necessary to shine extra light on the LDR. The same applies to the circuit that whistles upon illumination. To start the circuit it is necessary to distinctly illuminate the LDR.

2

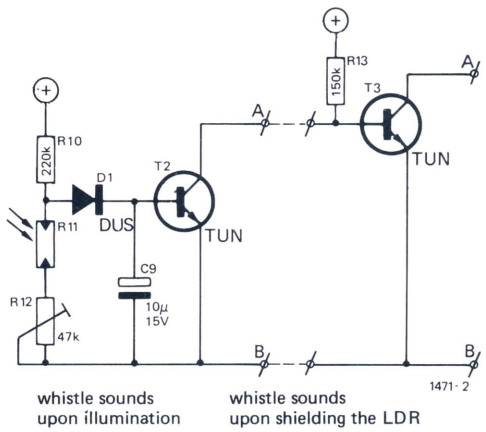
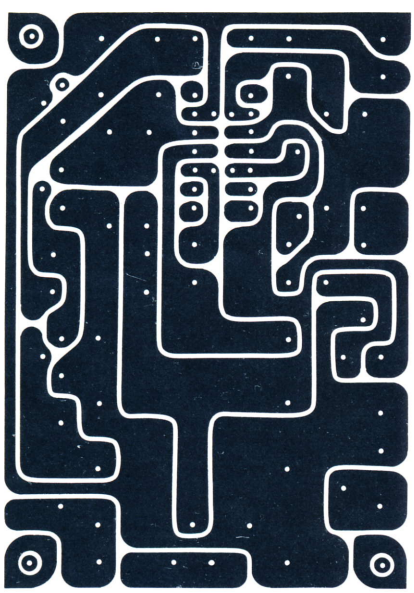
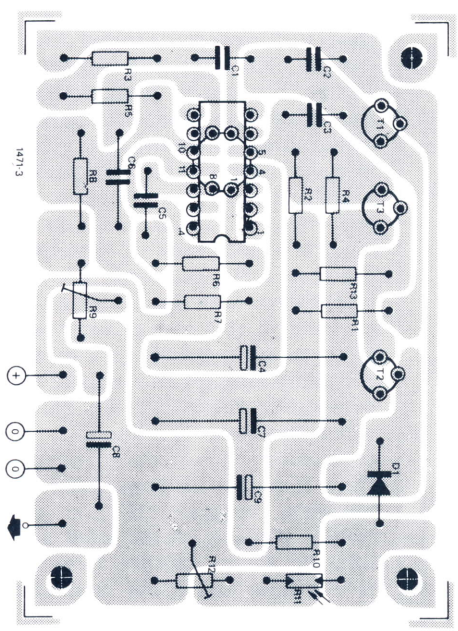


Figure 2. The optical keying switch for the steam whistle, which will respond to either illumination or shading of the LDR.

Figure 3. Printed circuit board and layout for the steam whistle with optical switch.

3





Parts list

Resistors:
R_1, R_2, R_4, R_8, R_{10} = 220 k
R_3 = 1k8
R_5 = 68 k
R_6 = 1k5
R_7 = 22 k
R_9 = 22 k, trimmer
R_{11} = LDR 03
R_{12} = 47 k, trimmer
R_{13} = 150 k

Capacitors:
C_1 = 0.033 µ
C_2 = 0.47 µ
C_3 = 0.27 µ
C_4 = 47 µ/15 V
C_5 = 470 p
C_6 = 22 p
C_7 = 500 µ, 16 V
C_8 = 1 µ, 15 V
C_9 = 10 µ, 15 V

Semiconductors:
T_1 ... T_3 = TUN
D_1 DUS
IC_1 = 709

mos-clock

(2)

The mos-clock described in this book can be extended with a crystal time base and an emergency supply. These do make the clock a bit more expensive, but they are at the same time elements changing the clock into a highly-accurate and universal instrument.
Furthermore, the total extra current consumed by these extensions is practically negligible. Both the emergency supply and the crystal time-base are mounted on one printed circuit board.

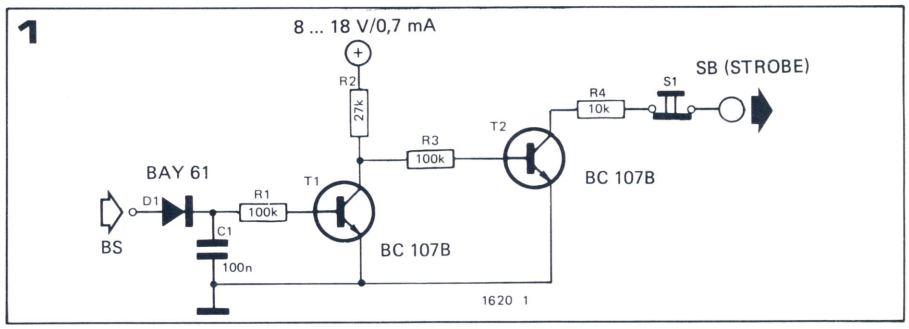
In recent years especially, the mains voltage has been liable to cut out momentarily (or even for quite some time!). Depending on the capacitance of the electrolytic in the power supply, the d.c. voltage driving the clock will have disappeared after about 200 ms. The clock will then forget what time it is, so that it must be reset. This is in itself not such an enormous problem, but a number of brief failures in one day could be annoying!
The emergency supply circuit described here uses a 9-volt battery. This provides an emergency drive for about 20 hours; a period within which even the most serious mains breakdown will have been repaired. The emergency drive also offers the possibility of moving the clock from one room to another without it stopping.

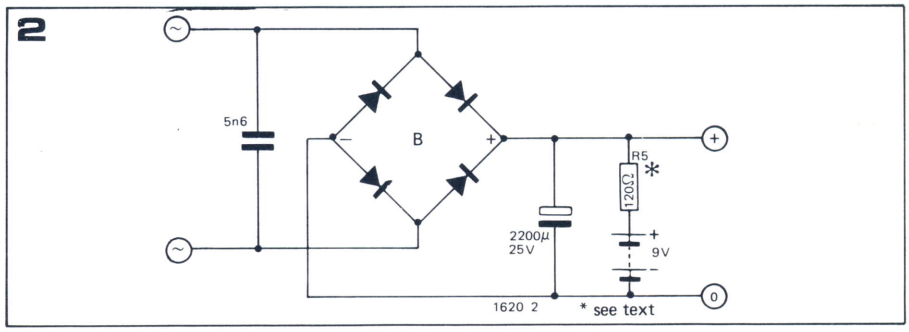
Design

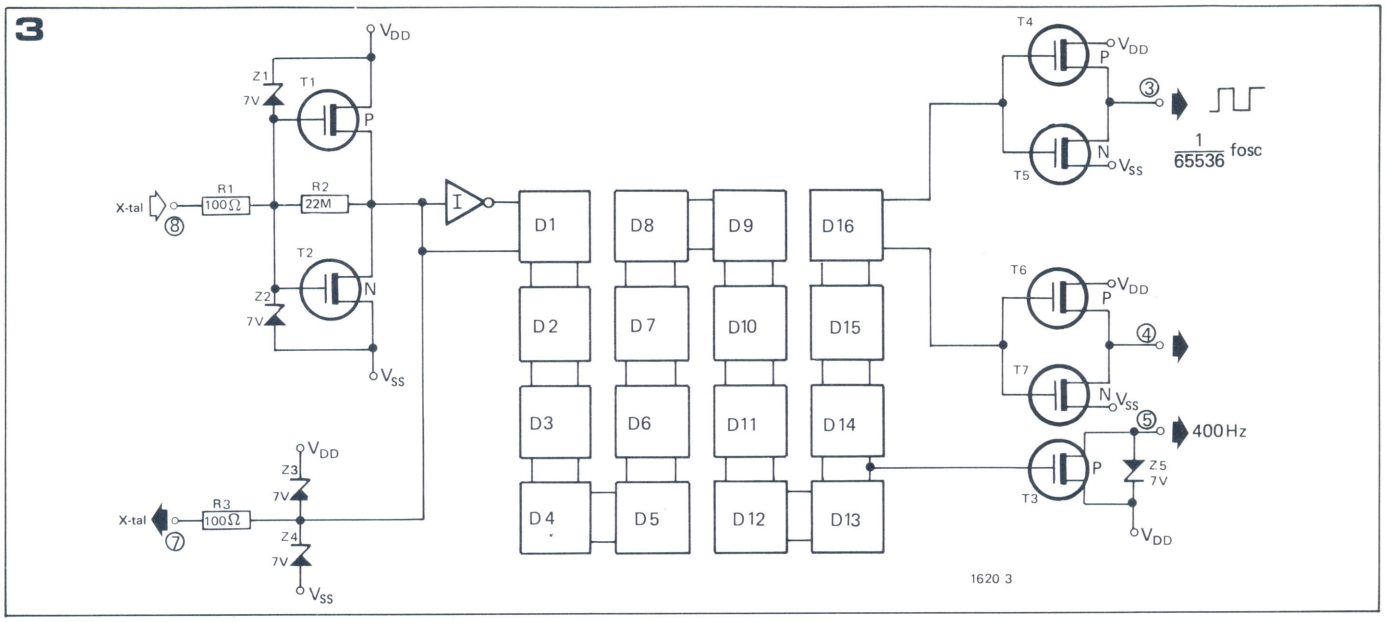
As the clock-IC MM5314 consists of one monolithic MOS circuit, its current consumption can be neglected in comparison with that of the displays. At 15 V the total current consumption of the clock is about 250 mA, 240 mA of which is drawn by the displays. This is one of the reasons why the clock-IC is provided with a so-called strobe input (pin 1 of the IC) which is '1' when the clock is running normally. If, however, the strobe input is made '0', the display is suppressed, and only the divider circuits and the memory still draw current.
These circuits still function satisfactorily at a supply voltage of 7 V.
So for an effective emergency supply from a small battery it is essential that as soon as the normal supply cuts out, the strobe input becomes '0' so that current consumption drops to about 8 mA. Of course, it must be possible to switch on the display circuits now and again on the emergency supply. A circuit which provides for this is given in figure 1.
If the mains voltage is available, the circuit is driven via point BS from the secondary of the transformer. This point is indicated on the clock P.C. board. The transformer secondary voltage on BS is rectified via D1, so that capacitor C1 is charged. Then transistor T1 is driven into saturation via resistor R1. The collector voltage of this transistor is then so low that transistor T2 is not driven. Via resistor R4 and push-button S1 the collector of T2 is connected to the strobe input of the clock-IC. This point (SB) is also indicated on the clock p.c.b. When transistor T2 is off, the strobe input of the clock-IC is connected to a relatively high-impedance load so that it 'sees' a '1', causing the displays to light up.
If, however, the mains voltage cuts out, point BS in figure 1 no longer carries a voltage, and C1 discharges so rapidly that transistor T1 is cut off within 5 ms. Now the base of T2 is driven via resistors R2 and R3, so that its collector-to-emitter resistance drops to about 200 ohms. As a result point SB becomes '0' via resistor R4 and the supply for the display circuits is cut off inside the clock-IC.

Figure 1. With the mos-clock, the displays draw most of the current. If the clock is provided with a circuit that drives the 'strobe' when the mains cuts out, the emergency battery will keep the clock itself running for about one day.

Figure 2. The mos-clock can easily be provided with an emergency supply. A 9-volt battery and a series resistance of 120 Ω will do.







When button S1 in figure 1 is depressed, the strobe input of the clock-IC becomes '1' again and the displays light up. Instead of a push button, a single-pole switch can be used for S1.

Practical version

For the emergency supply, only a battery with a series resistor need be connected across the supply electrolytic capacitor of the clock proper. Figure 2 shows the relevant detail of the clock supply: the extra battery and the series resistor R5 are in parallel with the supply elco. A so-called minipower pack will do as the battery. The design of the p.c.b. is based on this type of battery.

Two alternative arrangements are also possible. The first is to replace R5 by a diode, with the anode connected to the battery and the cathode connected to the supply rail. This has the advantage that the full battery voltage is available to drive the displays for short periods on emergency drive. However, it also means that no 'refresher' current runs through the battery when the mains is on.

Perhaps the best arrangement of all is to replace R5 by a diode, as above, and add an extra resistor of 100 k in parallel to the diode. This will trickle-charge the battery.

In all cases it is advisable to check the battery condition occasionally (by disconnecting the mains). This is particularly important when 'dry' batteries are used – they sometimes become very wet after a period of time, as many owners of portable radios and torches have discovered to their cost!

Crystal timebase

Although the standby supply will maintain the information in the memory of the clock in the event of a mains failure, the counting circuits will not operate in the absence of a 50 Hz signal. This is where the crystal timebase comes in. It ensures good timekeeping accuracy (approx. 10 seconds per month) and makes the drive to the clock independent of the mains.

Table 1. Some specifications of the Intersil IC type ICM 7038 A.

supply voltage	: 1.6 V . . . 4 V (max. 5 V)
current consumption	: 60 μA (V_b = 2.2 V); 130 μA (V_b = 3.6 V)
output resistance	: 230 Ω both for p- and n-output condition (I_o = 3 mA)
minimum oscillator frequency	: 0.2 MHz (V_b = 1.6 V)
maximum oscillator frequency	: 10 MHz
power dissipation	: 300 mW maximum
input voltage oscillator	: $\leqslant V_b$
case temperature	: −30° C . . . +125° C maximum
ambient temperature	: −20° C . . . +70° C maximum
output voltage	: $\approx V_b$ at all outputs
output current at V_o = 0	: 80 mA maximum
$V_o \approx V_b$	: 18 mA maximum
400 Hz output current ($V_a \approx V_b$)	: 30 mA maximum
400 Hz output resistance	: 200 Ω (I_a = 3 mA)

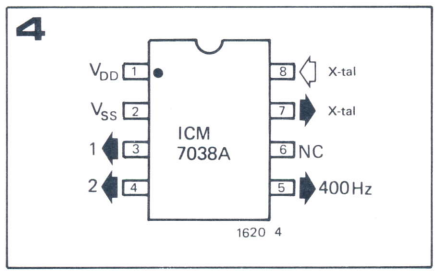


Figure 3. The intersil IC type ICM 7038 A comprises a.o. a 16-stage divider and a crystal oscillator. For the oscillator only the crystal and two capacitors need be connected externally. The IC is built up from complementary MOS-circuits, so that the power dissipation is extremely low.

Figure 4. The external connections of the ICM 7038 A. Owing to the COS/MOS properties, it is always advisable to use a base or socket for this IC.

Figure 5. The complete 50-Hz reference source for the mos-clock. The diodes D2 . . . D6 are for protection and ensure that the supply voltage for the IC cannot rise above about 3.5 V. T3 is needed because the output voltage of the IC is too low to drive the clock input directly.

Figure 6. The lay-out of the printed circuit board for the circuits of figures 1, 2, and 5.

Figure 7. The component arrangement on the printed circuit board of figure 6.

For this crystal time base use is made of a complementary MOS IC which, besides an oscillator, also comprises the dividers necessary for obtaining the 50 Hz square-wave voltage with which the clock is driven.

Figure 3 gives a simplified block diagram of this IC, the INTERSIL ICM 7038 A. Transistors T1 and T2 in figure 3 are a part of the crystal oscillator. Two external capacitors and the crystal are connected between points 7 and 8. The oscillator is followed by an inverter (I) which is turn is followed by 16 divider stages. The 16th divider is followed by two inverse output stages at which a relatively low-impedance square-wave voltage is available for further processing. The divider stages D1 . . . D16 are all binary so that after the 16th divider we have a frequency of:

$$f = f_o/2^{16} = f_o/65536$$

Here f_o is the oscillator frequency and f the output frequency behind the 16th divider.

It is also apparent from figure 3 that all important points are protected by means of zener diodes. This does not imply, however, that the IC can be handled as if it were TTL: due care is always recommended. Touching the connecting pins of the IC must be avoided as much as possible, whilst the IC can best be mounted on the p.c.b. by means of a socket.

The most important specifications of the ICM 7038 A are given in table 1. The low supply voltage (1.6 . . . 4 V) and the low current consumption (average 90 μA) are worthy of note. Figure 4 gives the pin connections of the ICM 7038 A.

The circuit

Figure 5 shows the circuit diagram of the complete time base.

Since the clock supply lies between 8 V and 18 V, a special circuit must be provided which ensures that the time base IC gets no more than 5 V. The simplest solution is shown in figure 5: the IC is fed via a resistor R6, and an electrolytic capacitor (C4) is connected across the IC. The diodes D2 . . . D6 ensure that the supply voltage can never rise above about 3.5 V.

In figure 5 the capacitors C2, C3 and the crystal are the external components

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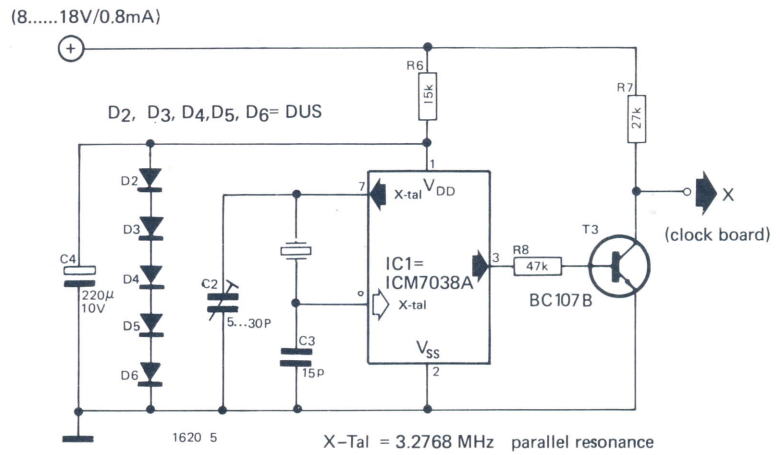

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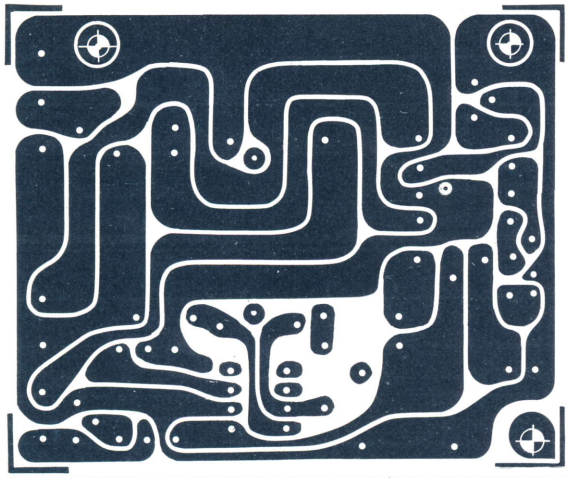

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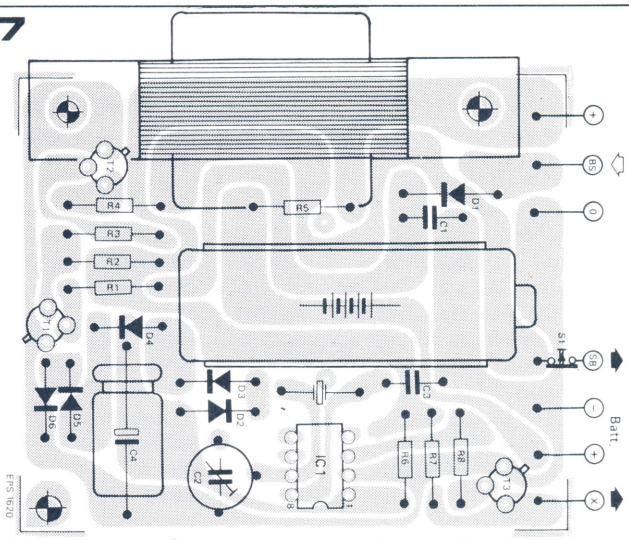


for the oscillator. The crystal must be of a type that has been ground for parallel resonance with an external parallel capacitance of 12 pF nominal. For 50 Hz output reference the crystal frequency must be 3.2768 MHz. The oscillator can be adjusted with capacitor C2.

Transistor T3 has been included in the circuit to make the output voltage of IC1 suitable for clock drive. The collector of this transistor is connected to point X on the clock p.c.b., after which resistor R22 (100 k) is removed.

The printed circuit board

Figure 6 shows the lay-out of the printed circuit board on which the circuits of figures 1, 2 and 5 can be mounted. The component arrangement of these circuits is given in figure 7.

Figure 8 shows a photograph of the board. It can be mounted on the mains transformer on the original clock board.

Parts list for figures 1, 2, 5, and 7.

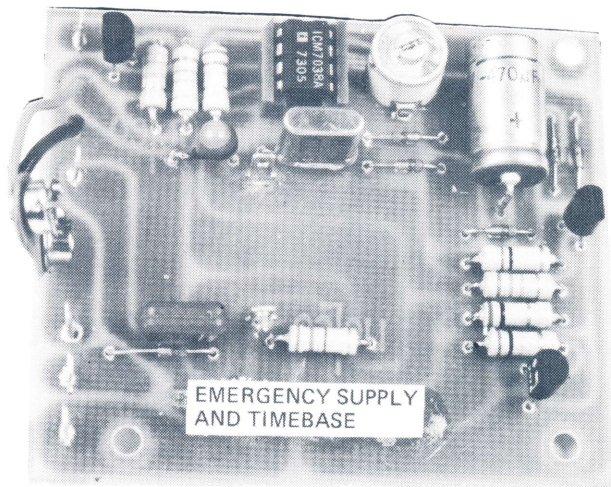
resistors:
R1,R3 = 100 k
R2,R7 = 27 k
R4 = 10 k
R5 = 120 Ω
R6 = 15 k
R8 = 47 k

capacitors:
C1 = 0.1 μ
C2 = 5 . . . 30 p trimmer
C3 = 15 p
C4 = 220 μ, 10 V

semiconductors:
T1,T2,T3 = BC 107 B or equ.
D1 = BAY 61, BA 127
D2,D3,D4,D5,D6 = DUS
IC1 = ICM 7038 A (intersil)

miscellaneous
S1 = push button with break contact
X-tal = 3.2768 MHz crystal; parallel resonance with external 12 p
8-pin DIL IC-base for IC1

8



edwin amplifier

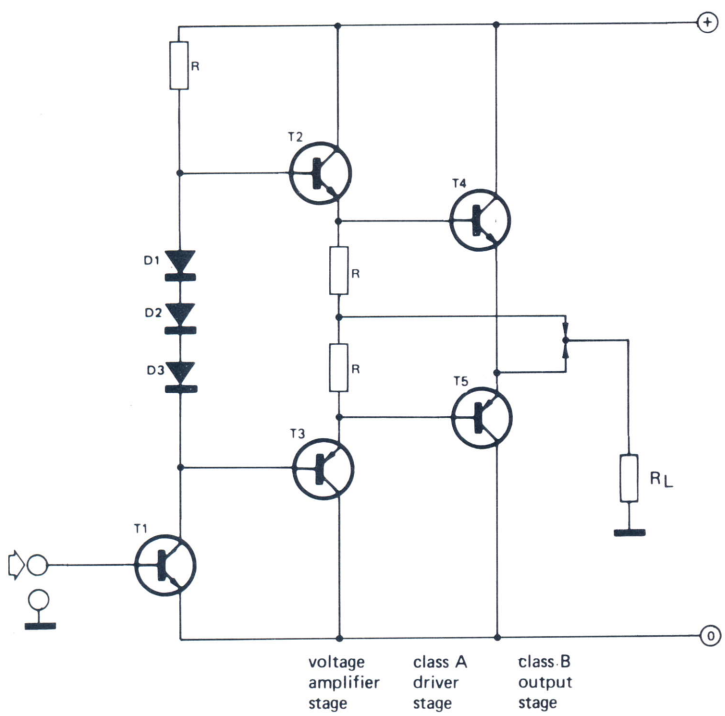
This is a design for a high-quality 40 W audio amplifier based on an earlier 20 W design which has proved very popular on the continent. The amplifier embodies some unusual design features and the construction is problem-free due to the small amount of negative feedback employed and to the absence of quiescent current in the output stage.

The Edwin amplifier is unusual in that it embodies two types of output stage in one amplifier. A class A output stage handles the low level signals and also serves as a driver for a class B stage which handles the larger outputs.
The principle of operation is shown in figure 1. T2 and T3 are biased on by the voltage drop across the diodes D1-D3. T2 and T3 function as a class A stage at low signal levels supplying current to the load via resistors R. As the signal is increased the voltage drop across these resistors becomes sufficient to cause T4 and T5 to conduct and the class B part of the output stage begins to operate. Crossover distortion is quite low with this type of design.

The complete circuit

As figure 2 shows, the complete amplifier circuit consists of a voltage amplifier, a class A driver stage and a class B output stage. The input stage consists of T1 and T2 in a Darlington configuration, resulting in a high input impedance. The signal passes to the base of T3 via the limiting resistor R4. T3 operates as a voltage amplifier and in its collector circuit has T4, which is connected as a simulated zener diode to provide a constant d.c. bias voltage of about 2 V across the bases of the driver transistors T7 and T8. Feedback is applied between the output and the junction of R11 and R12 to provide a high collector impedance so that true current drive is achieved. This helps to reduce crossover distortion still further so that despite the small amount of overall negative feedback and the absence of quiescent current in the output stage the distortion figures are very good.

1



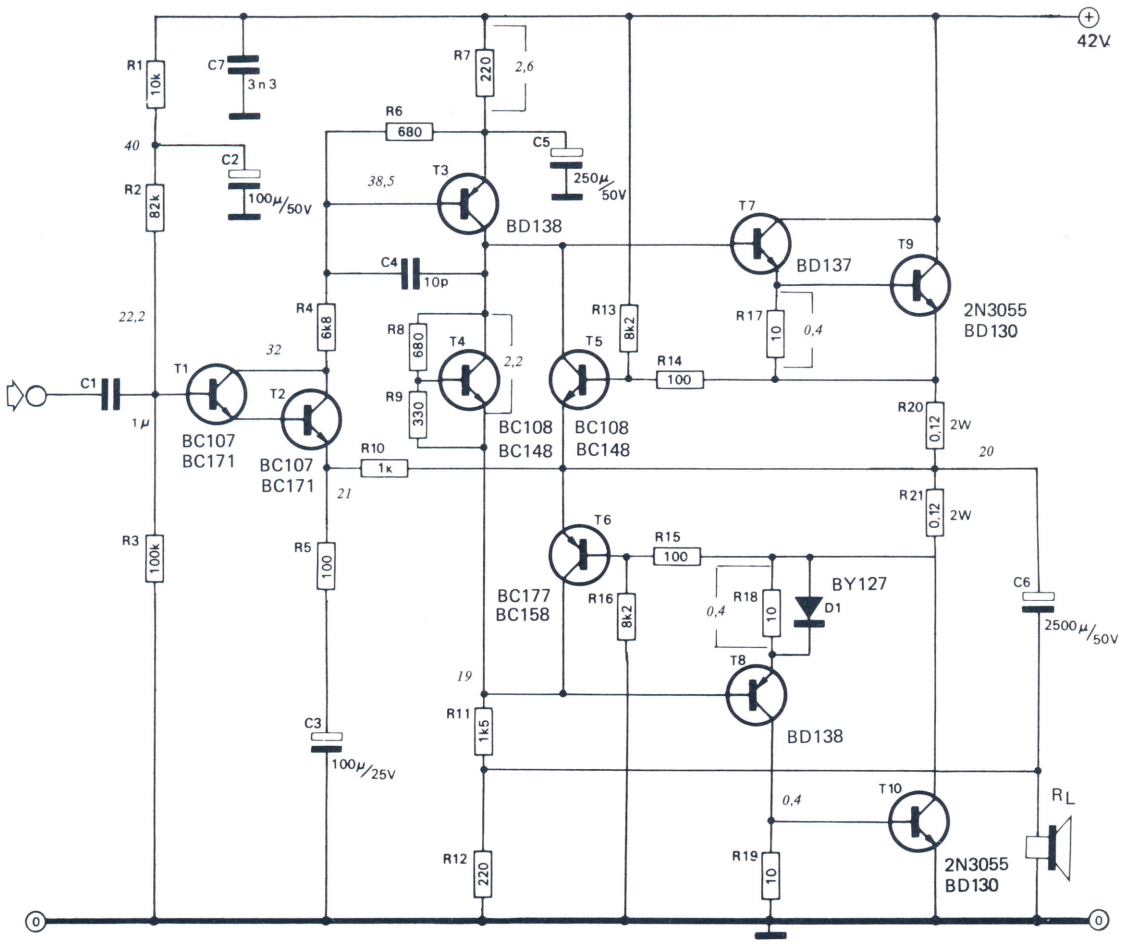
features

- output power from 10-40 W depending on power supply.
- high efficiency.
- low crossover distortion.
- short circuit proof.
- no quiescent current in the output transistors.
- output transistors and drivers need not be matched.
- unconditionally stable.

figures

- Sensitivity: ≈ 1 V (RMS).
- Input impedance: ≈ 45 kΩ.
- Distortion: 1 kHz, 30 W: 0.1%, 10 kHz, 30 W: 0.3%.
- Power bandwidth: 20 Hz – 100 kHz.
- S/N ratio: > 90 dB.

2



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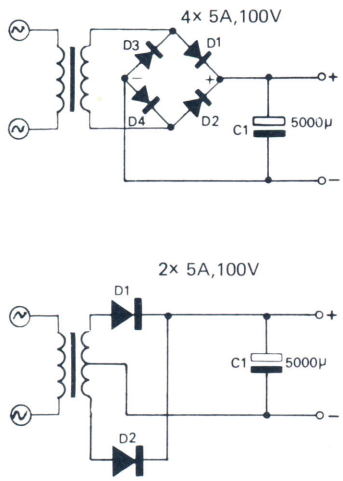

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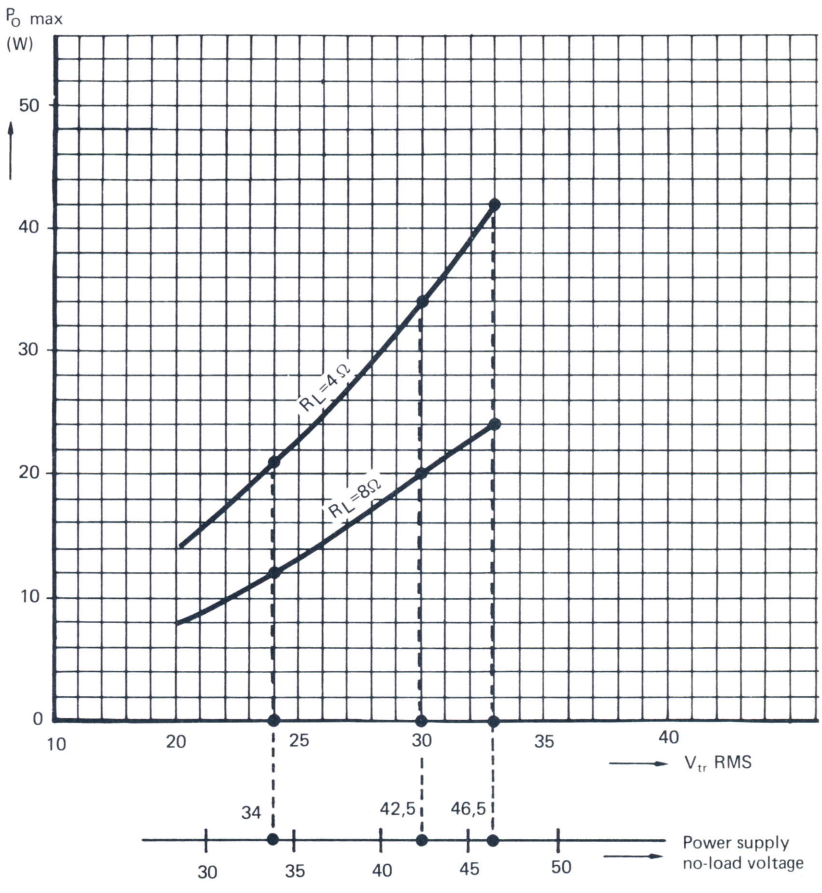
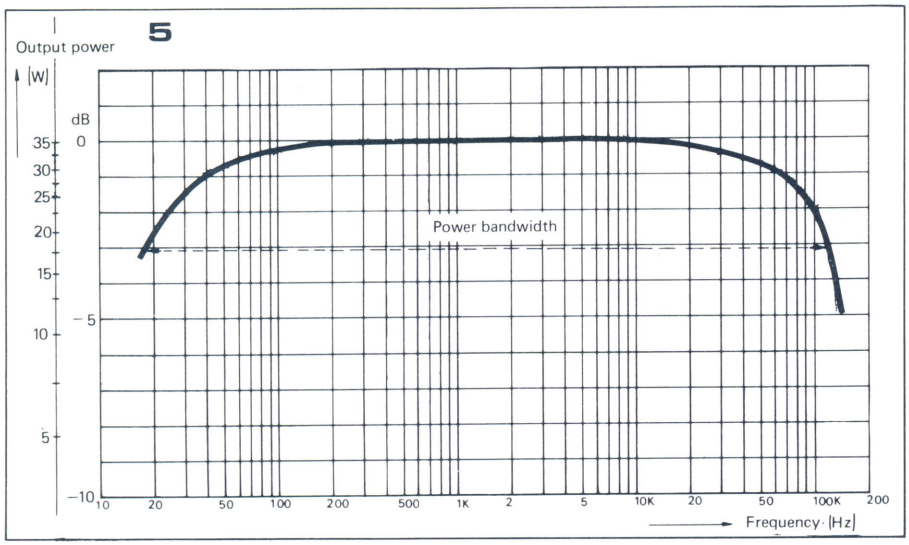


Figure 1. Basic circuit of an Edwin-type output stage.

Figure 2. Final circuit of the Edwin amplifier for output powers up to 40 W.

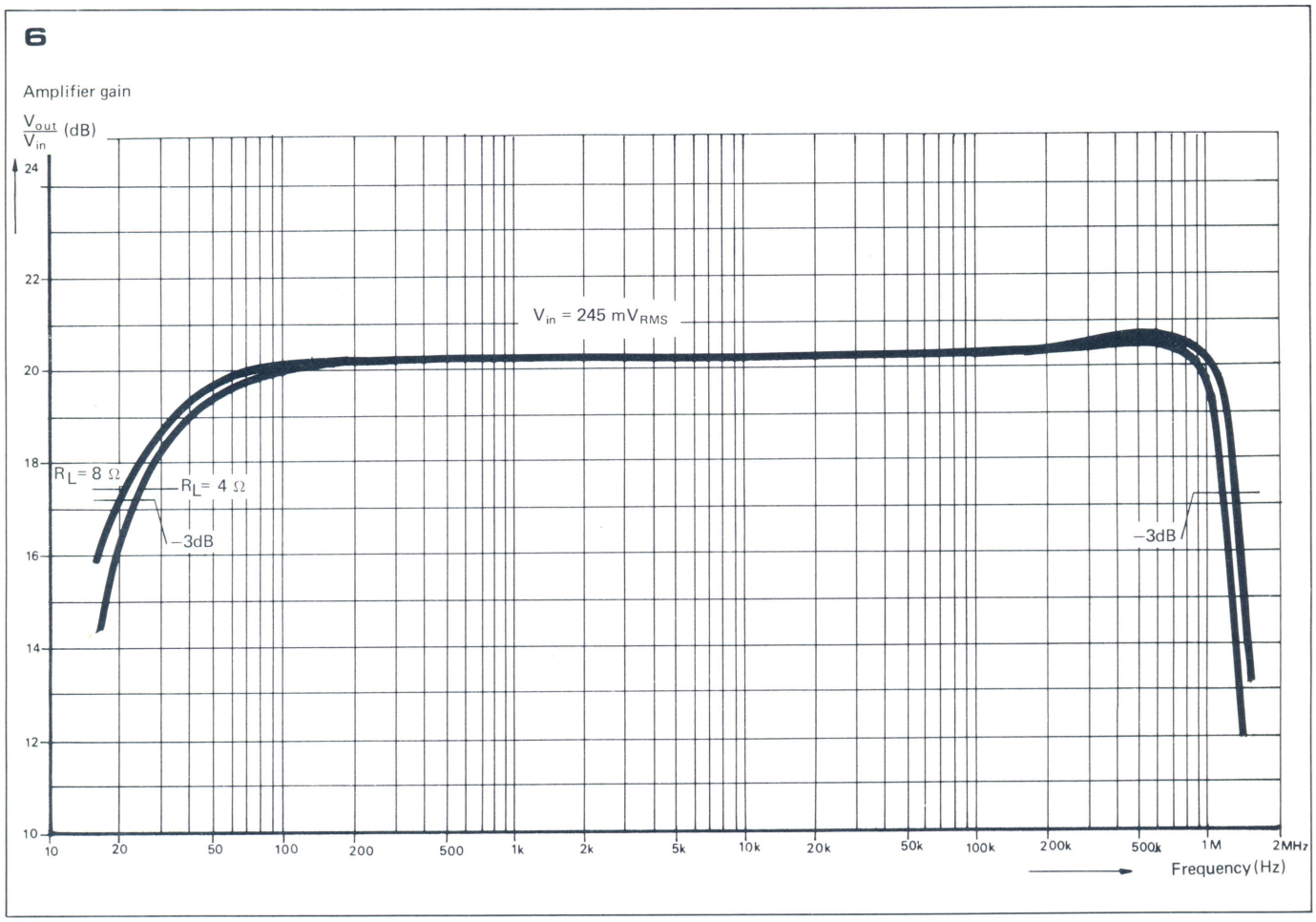
Figure 3. The power supply.

Figure 4. Graph of available output power versus transformer secondary voltage for 4 Ω and 8 Ω loads.



The output stage differs from the configuration shown in figure 1 because it comprises two NPN transistors of the same type and not a complementary pair. To maintain symmetrical operation of the output stage D1 is included across R18. This simulates the base-emitter junction which would be present across R18 if the configuration of figure 1 has been used. The values of R17, R18 and R19 are low (10 Ω) to reduce cross-over distortion.

Overall negative feedback is applied from the output to the emitter of T2. The inclusion of C3 means, that 100% d.c. feedback is applied, which stabilises the d.c. operating point of the output at around half supply voltage over a wide range of supply voltages without the need for adjustment potentiometers.



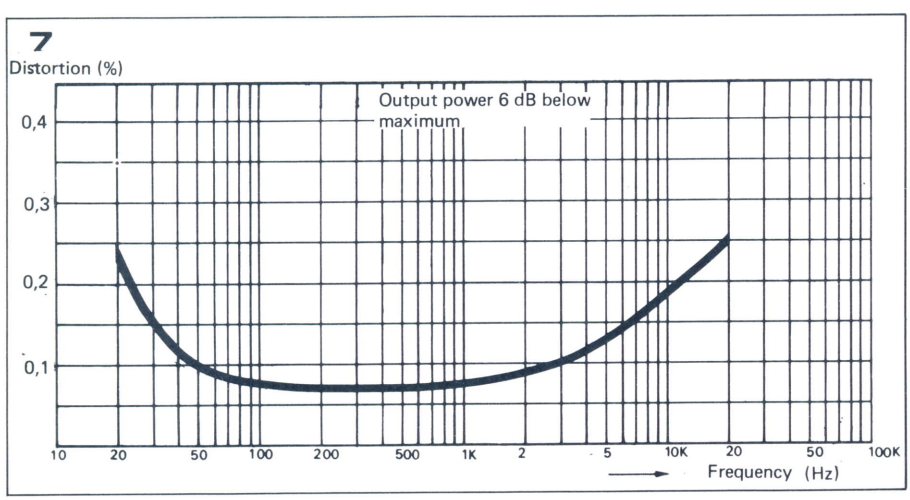


Figure 5. Maximum output power versus frequency.

Figure 6. Frequency response.

Figure 7. Distortion versus frequency for output power 6 dB below maximum.

Figure 8. Distortion versus output power.

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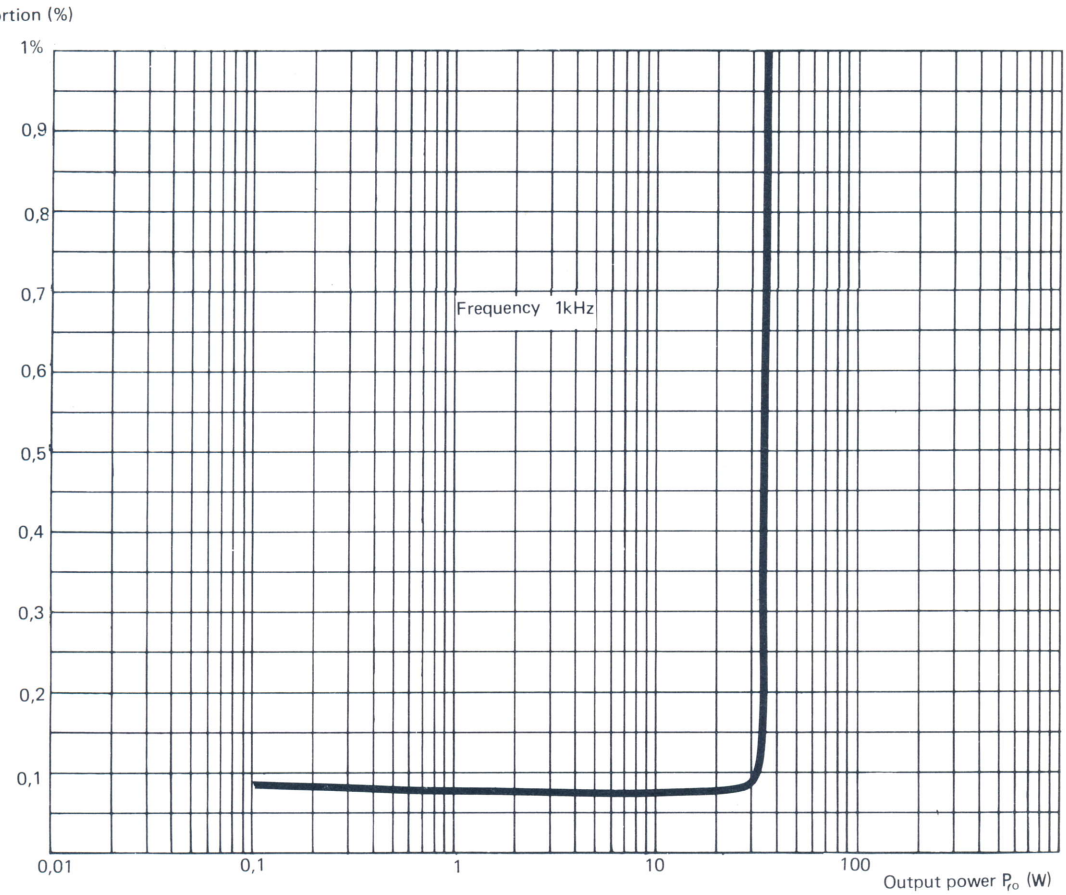


The a.c. gain of the amplifier is, of course, given by

$$A_V = \frac{V_{out}}{V_{in}} = \frac{R_{10} + R_5}{R_5}.$$

It is worth noting the effect of the combination R7, C5 on the operation of the amplifier. Some amplifiers, when used with an unstabilised supply, display ripple on the peaks of the waveform when driven to clipping. This is eliminated by R7 and C5 as follows. When the amplifier is being driven, current flows through R7 and the voltage on C5 is always below the ripple 'troughs' on the supply. The drive voltage available from T3 is limited to the voltage on C5 and the output of the amplifier can never swing into the ripple region of the supply voltage. R7 also limits the current through T3 in the event of an overload.

Overload protection

The protection circuit is designed to prevent excessive current peaks from occurring during signal overloads or short-circuiting of the output. The protection circuit consists of transistors T5 and T6. Their base bias is set such that under normal operating conditions the voltage across R20 and R21 is insufficient to turn them on. In the event of excessive output current flowing in R20 or R21, due to a signal overload or a short-circuited output, the voltage across these resistors is sufficient to cause T5 or T6 to conduct. This reduces the drive voltage to the output stage and therefore limits the output current, thus protecting the amplifier.

Power supply

A stabilised power supply is unnecessary with the Edwin amplifier, as its performance will not be significantly improved. A simple unregulated supply is quite adequate and two suitable circuits are given in figure 3. Figure 3a shows a supply using a normal full-wave bridge rectifier, whilst figure 3b shows a full-wave rectifier with a centre-tapped transformer.

The component values and specification for supplies suitable for 20, 35 and 40 W versions of the amplifier are given in table 1. Of course any suitable transformer may be used, there is no need to adhere to the exact voltages specified. Figure 4 gives the output power available versus transformer secondary voltage. The only points to watch are that the current rating of the transformer is adequate for the required output power, that the voltage rating of the smoothing capacitor is sufficient and that the RMS secondary voltage of the transformer does not exceed 33 V on load, otherwise the voltage rating of the transistors may be exceeded.

Over the range of supply voltages given in figure 4 nothing need be changed in the amplifier as the operating point is self-adjusting.

Performance figures

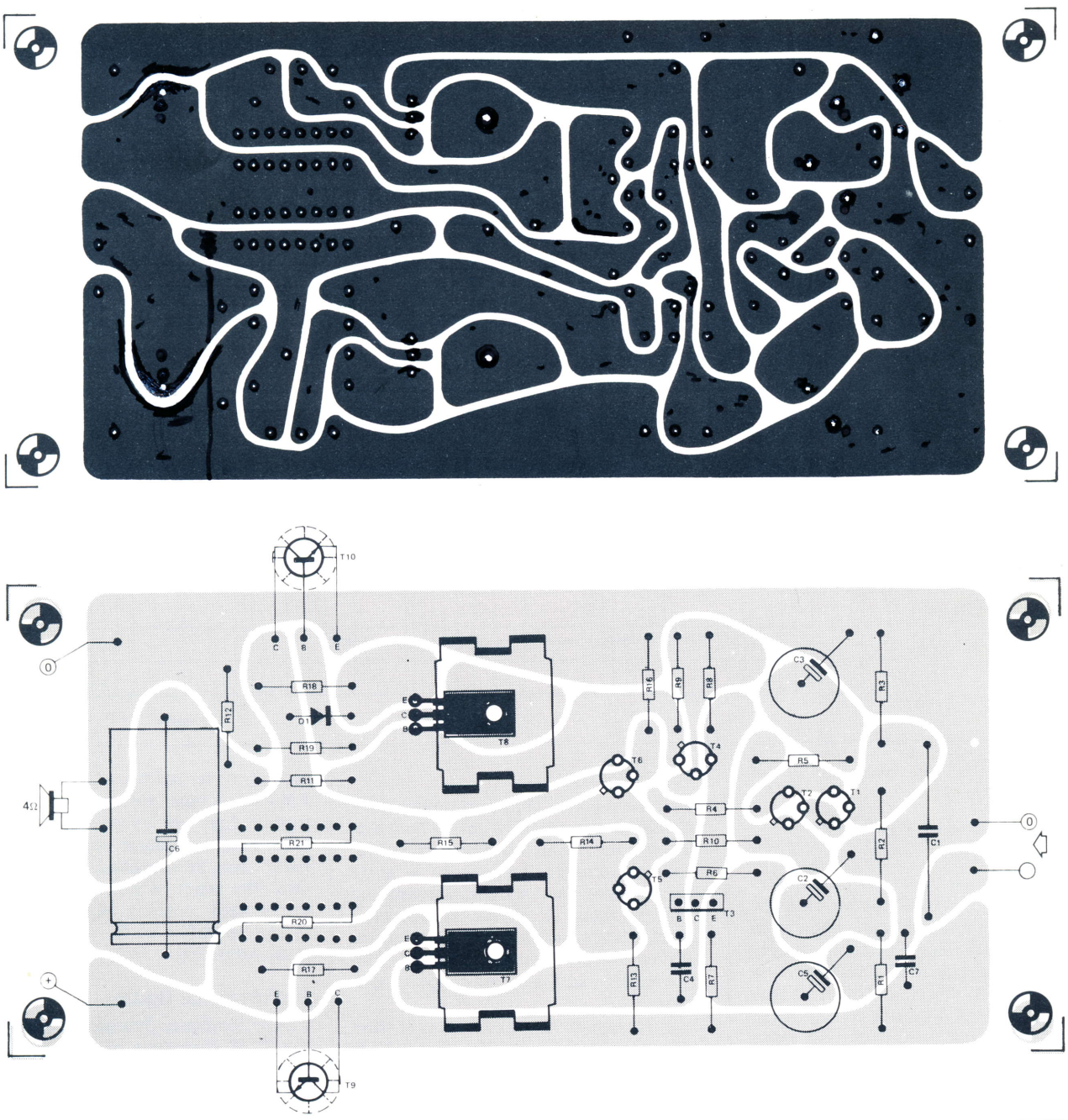
The performance figures, as measured on the 35 W prototype of the amplifier are summarised in table II and displayed graphically in figures 5, 6, 7, and 8. As can be seen they are quite exceptional. Among the outstanding features are the large power bandwidth, good signal to noise ratio, immunity to transients, low distortion and absolute stability, even with large capacitive loads.

Figure 9 shows the printed circuit board and component layout of the amplifier.

Table I

P_o max (W) (R_L = 4 Ohm)	V_{tr} RMS	I_{tr} max (A) figure 3b Mono	figure 3b Stereo	figure 3a Stereo	C1 µF Mono	C1 µF Stereo	C1 working voltage (V)	Power supply no-load voltage (V)
42	33	1,1	2,2	4,5	2500	5000	60	46,5
35	30	1	2	4			50	42,5
21	24	0,8	1,5	3			40	34

9



Components list for figures 2 and 9

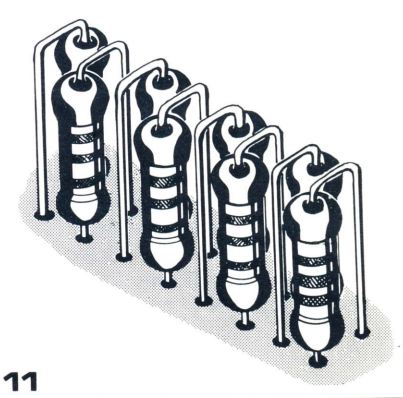
Resistors:
R1 = 10 k, ¼ W
R2 = 82 k, ¼ W
R3 = 100 k, ¼ W
R4 = 6k8, ¼ W
R5,R14,R15 = 100, ¼ W
R6,R8 = 680, ¼ W
R7,R12 = 220, ¼ W
R9 = 330, ¼ W
R10 = 1 k, ¼ W
R11 = 1k5, ¼ W
R13,R16 = 8k2, ¼ W
R17,R18,R19 = 10, ¼ W
R20,R21 = 0.12, 2 W

Capacitors:
C1 = 1 μ
C2 = 100 μ, 50 V
C3 = 100 μ, 25 V
C4 = 10 p ceramic
C5 = 250 μ, 50 V
C6 = 2500 μ, 50 V
C7 = 3n3

Semiconductors:
T1,T2 = BC 107, BC 171
T4,T5 = BC 108, BC 148
T3,T8 = BD 138
T6 = BC 178, BC 158
T7 = BD 137
T9,T10 = 2N3055, BD 130
D1 = BY 127

Figure 9. Printed circuit board and component layout.

Figure 10. Heatsink details for the driver and output transistors.



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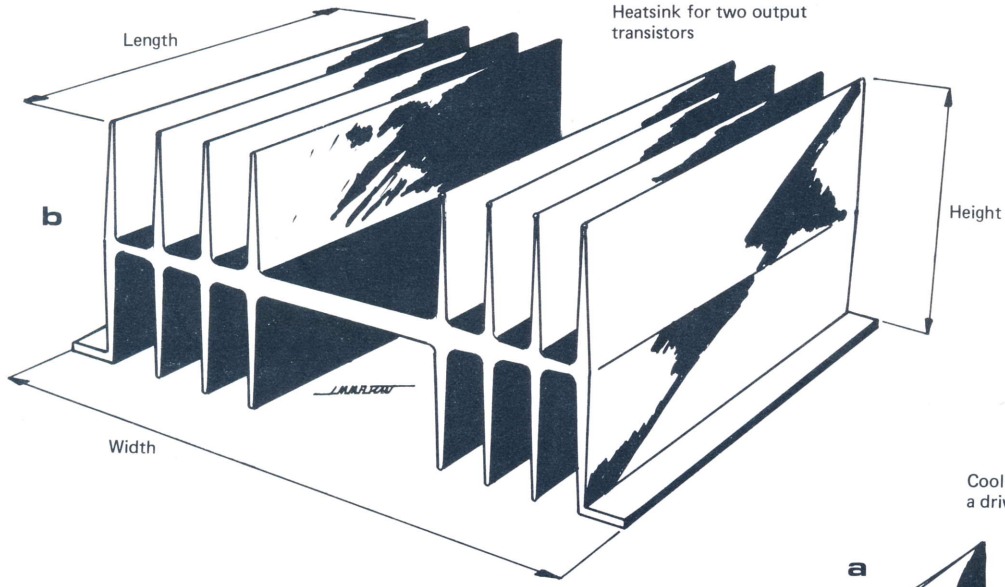
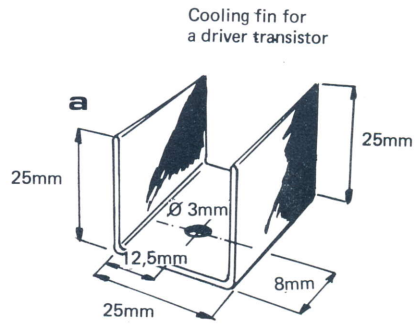


P_o max.	W	H	L
42Watt	approx. 100mm	approx. 60mm	approx. 75mm
35Watt			
21Watt			50mm



The driver transistors are mounted on the board, with a cooling fin as detailed in figure 10a. The output transistors are mounted on a separate extruded aluminium heatsink, details of which are given in figure 10b and the associated table. Most manufacturers of heatsinks will have something similar to this in their range.
If resistors R20 and R21 are not readily obtainable they may be wound from suitable resistance wire. Alternatively wire eight 1 Ω 0.25 W resistors in parallel, there is plenty of space on the board to mount them vertically (figure 11).

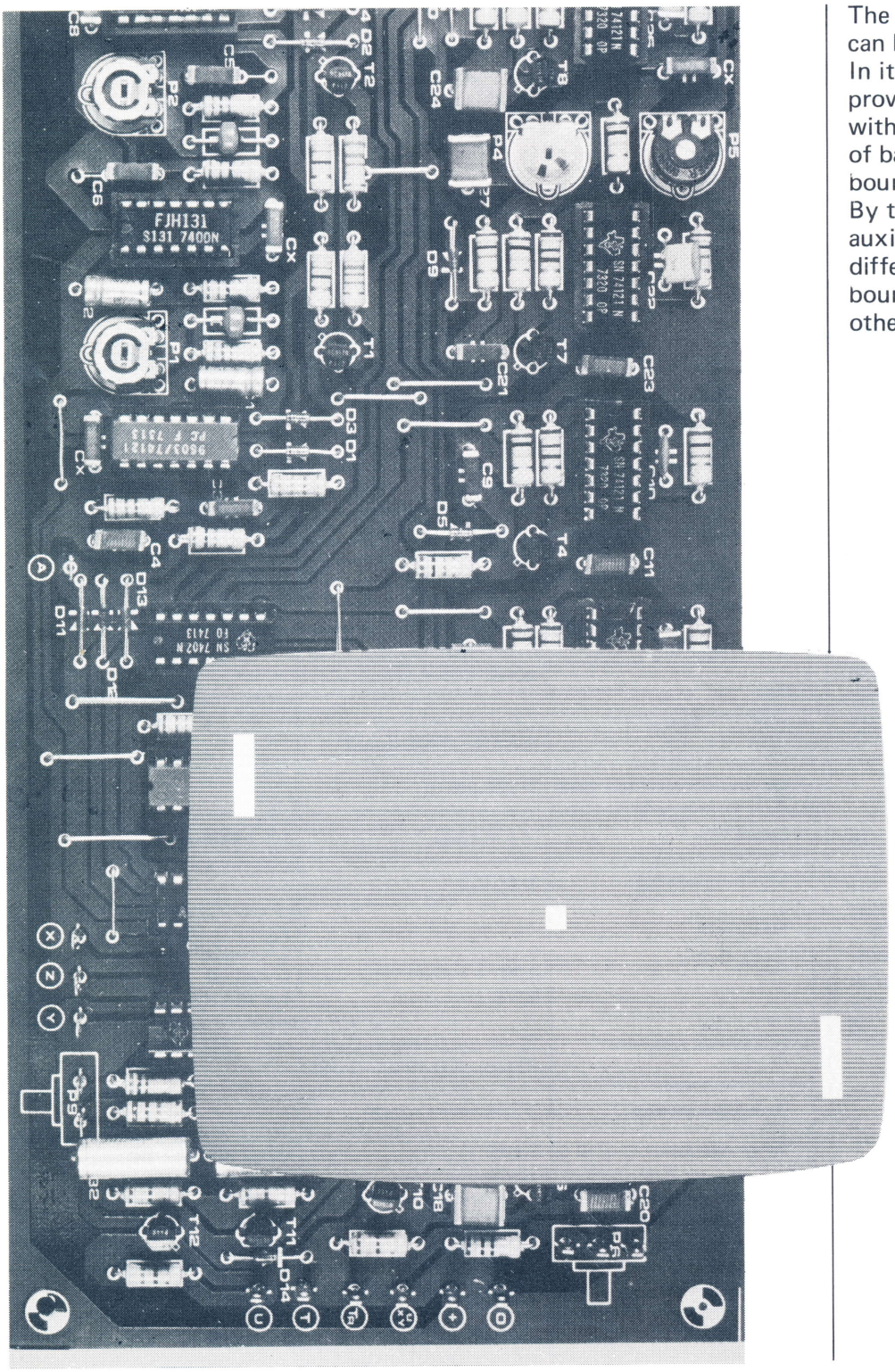
Concluding remarks

Whilst the Edwin amplifier meets an exacting specification this is no reason to recommend its construction by the Hi-Fi enthusiast. There are many other designs with similar performance. What makes the amplifier eminently suitable for the amateur is its problem-free construction and virtual (electrical) indestructibility. ◀

Table II

Performance figures of 35 W version		
Maximum output power	35 W (4 Ω); 20 W (8 Ω) 45 W (4 Ω); 27 W (8 Ω)	f = 1 kHz, THD = 1 % THD = 10%
Efficiency	> 60%	f = 1 kHz; P_o = 35 W
Load impedance	0 ... ∞ (Maximum power into 4 Ω)	
Overload protection	Proof against long duration short-circuit	
Maximum capacitive load	> 100 μF (!)	
Sensitivity	≈ 1 V RMS	f = 1 kHz, P_o = 35 W
Input impedance	≈ 45 kΩ	
Distortion	0,1% 0,2% 0,3%	P_o = 0 ... 30 W f = 1 kHz f = 30 Hz f = 10 kHz
Frequency response	25 Hz ... 1,2 MHz (−3 dB) 40 Hz ... 1,0 MHz (−1 dB)	V_{in} = 245 mV
Power bandwidth	> 100 kHz (−3 dB)	
Noise rejection	73 dB 93 dB	input open-circuit input short-circuit
Signal to noise ratio	95 dB > 105 dB	input open-circuit input short-circuit
Feedback factor	≈ 36 dB	
Stability	unconditional	

TV Tennis extensions



The scope of the TV-tennis game can be considerably extended. In its basic form the circuit provides only the tennis game, with a display consisting simply of bats and ball, with no boundaries or other refinements. By the addition of a number of auxiliary circuits, a number of different games can be played, and boundaries, automatic scoring and other effects can be added.

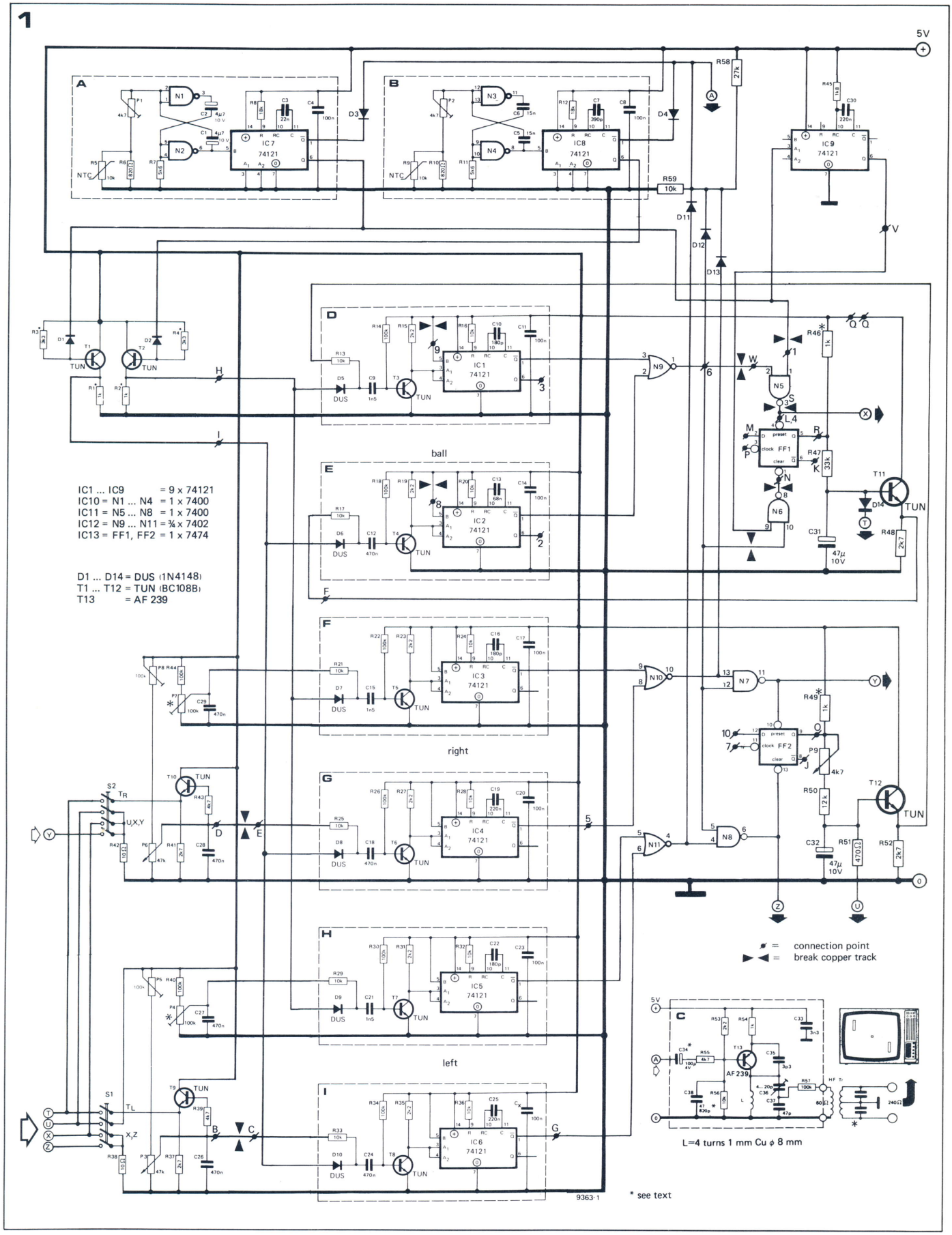


Figure 1. The original circuit of the TV tennis game. The new connection points and the places where connections will have to be broken are shown.

The extensions to the TV tennis game are connected into various points on the existing board. In some cases the track on the existing board must be broken for connection of the auxiliary circuit. Figure 1 gives details of these modifications to the existing board. In the course of the article it will be made clear which connection points are used for the various extensions to the game.

Automatic opponent

TV tennis, like may other pastimes, is

a game that only two can play. However, for solo practice it is a relatively simple matter to provide an automatic opponent, who never gets tired and who never misses a shot. This is accomplished by making the vertical position of the automatic opponent's bat always coincide with the position of the ball. Vertical control of the bat must therefore be disconnected from the player controls (P3 or P6) and must be connected to the vertical ball position control. To do this the connections to the sliders of P3 and P6 from R33 and R25 must be broken, giving 4 new connection points:

B : slider P3/C26/R39
C : left-hand side R33
D : slider P6/C28/R43
E : left-hand end R25

A new connection is also made to the emitter of T11 (F). An auto/manual switch is connected to these points so that point C may be switched between points B and F, and similarly a switch is introduced between points E, D and F (figure 3).

Vertical Centre Line

It is usual with most ball games to have the field of play divided into two halves. A vertical centre line will serve as the net for TV tennis, or as the centre line for a football game, which will be described later. A white centre line is easily achieved by producing a peak white video pulse halfway along each line sweep. The circuit that performs this function consists of a delay circuit triggered from the line sync pulses, and a monostable to produce the pulse (figure 4). This is almost identical to the circuits used in the original design for the generation of the bats and ball. The circuit is triggered from point H (emitter of T2), and the output is taken to the video mixer (point A). The horizontal position of the line may be adjusted by varying the delay with P10.

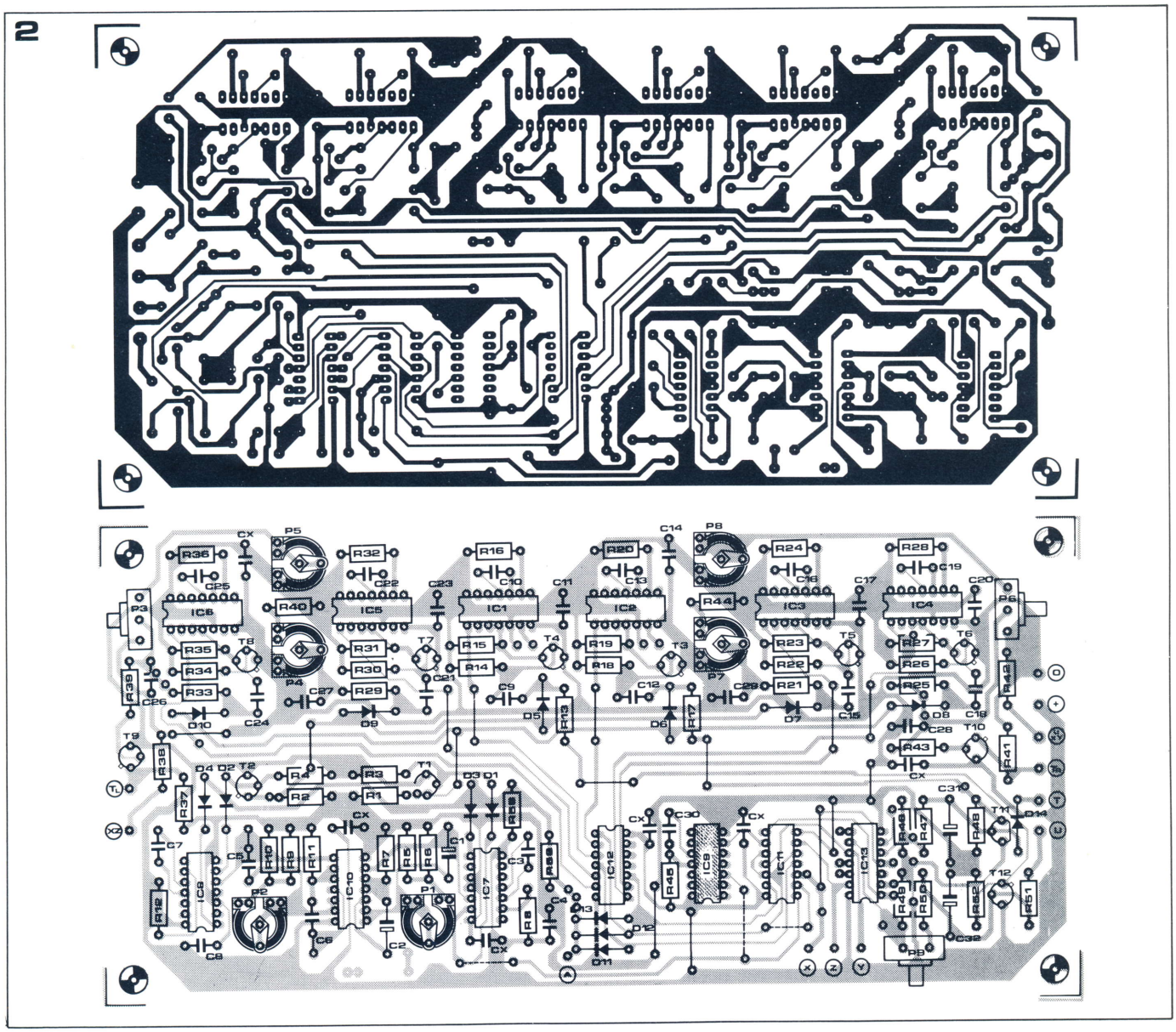
Vertical boundaries

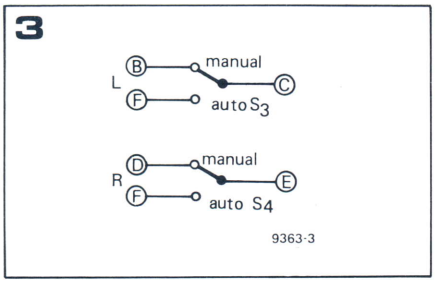
In the basic version of the TV tennis game the vertical boundaries at the top and bottom of the picture, from which the ball rebounds, are invisible. Since one of the boundaries is derived from the field sync pulses and occurs during the field blanking interval, the ball may disappear from the screen for short periods. It is much more pleasing if the ball can be seen to rebound from a visible (white) barrier.

To give horizontal white boundaries at the top and bottom of the picture it is necessary to produce a peak white video signal that lasts for several line periods, and overlaps the start and finish of the field sync pulse. The portion of the video pulse before the field sync pulse produces the lower boundary, and the portion after produces the upper boundary. This is shown in the timing diagram of figure 5. The video pulse is again produced by a delay circuit and monostable (figure 6), but here the delay is triggered from the leading edge of the field sync pulse. This entails connecting the input of figure 6 to point I (emitter T1). The output again goes to the video mixer.

P11 adjusts the delay, and therefore the position of the boundaries, while P12 adjusts the duration of the video pulse, and hence the width of the boundaries.

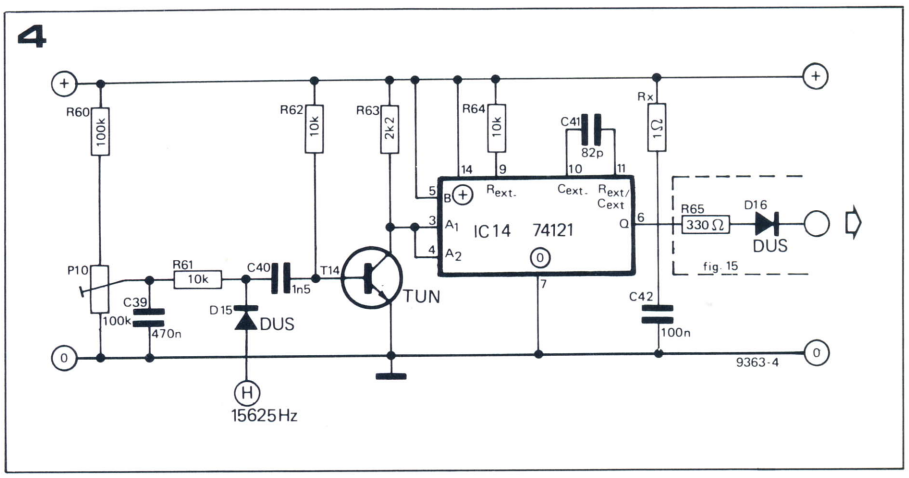
As the ball must now rebound from these new boundaries, the connections to FF1, which determines vertical ball direction in the original circuit, must be somewhat modified. The new connec-

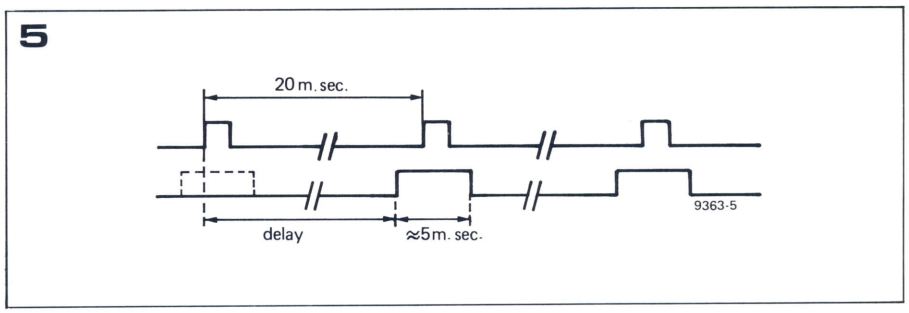


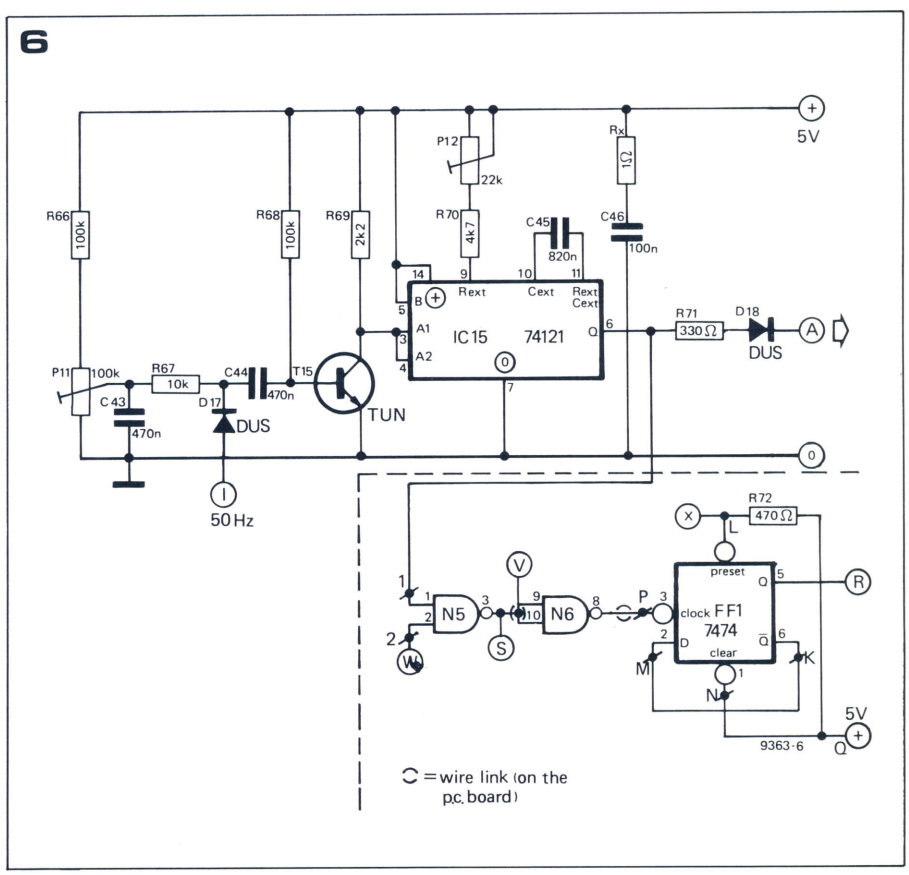


tions are shown enclosed in the dotted box in figure 6. Instead of functioning as a set-reset flip-flop, FF1 is now connected in the divide-by-two mode, so every time a pulse reaches its clock input it changes state. The pulses to trigger the flip-flop are obtained from the output of N6, N5 and N6 being connected to form an AND gate. When the vertical ball signal (Q output of IC2 connected to point W) and the Q output of IC15 are both '1' this indicates a coincidence between the ball and the upper or lower boundary, so the output of N6 will become '1' and FF1 will change state, reversing the vertical ball direction.

The preset input of FF1 is still connected to point X of the original circuit,







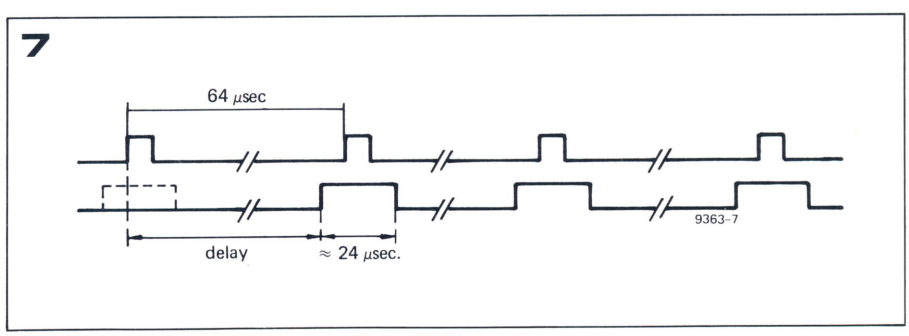


Figure 2. Half-size reproduction of the main board and component layout. (Shown full-size on pages 32 and 33).

Figure 3. The automatic opponent is very simple to add: two single-pole double throw switches are all that is required.

Figure 4. The centre line. As in the rest of the circuit, a combination of pulse delay and monostable multivibrator is used for this.

Figure 5. Pulse diagram of the horizontal boundaries. Approximately 18 msec after each frame sync pulse a 5 msec pulse is produced, which overlaps the next frame sync pulse.

Figure 6. Circuit for producing the horizontal boundaries. This extension entails modifying part of the original circuit, as shown in the lower half of the diagram. IC9 must be removed from the original board.

Figure 7. Pulse diagram for the vertical boundaries.

but is no longer connected to the output of N5. Instead, a 470 Ω pullup resistor is connected from this point to the positive supply. The connections to the Q output of FF1 (R46/R47) remain unchanged.

To recap, the modifications to this part of the circuit are as follows:

1. tracks connected to the inputs and outputs of N5 and N6 are broken.
2. Pin 2 (point W) of N5 is connected to pin 6 (point 2) of IC2. Pin 1 (point 1) of N5 is connected to pin 6 of IC15 (on new ancillary board). Pin 3 (point S) of N5 is connected to pins,9 and 10 (point V) of N6.
3. Pin 8 of N6 is connected to pin 3 (point P) of FF1. Pins 2 and 6 (M and K) of FF1 are linked, and pins 1 and 4 (N and L) of FF1 are linked by the 470 Ω resistor. Pin 1 is also connected to +5 V by joining it to pin 14.
4. IC9 is now redundant and may be removed from the board.

These modifications may be carried out by means of wire links on the back of the board.

Left and Right Hand boundaries

A further logical extension to the TV tennis game is the addition of vertical white bars as boundaries at the left- and right-hand extremes of the 'court'. If automatic scoring is to be incorporated these are essential. When the ball crosses one of these boundaries this indicates that a point has been scored, and the signal required to trigger a points counter can easily de derived.

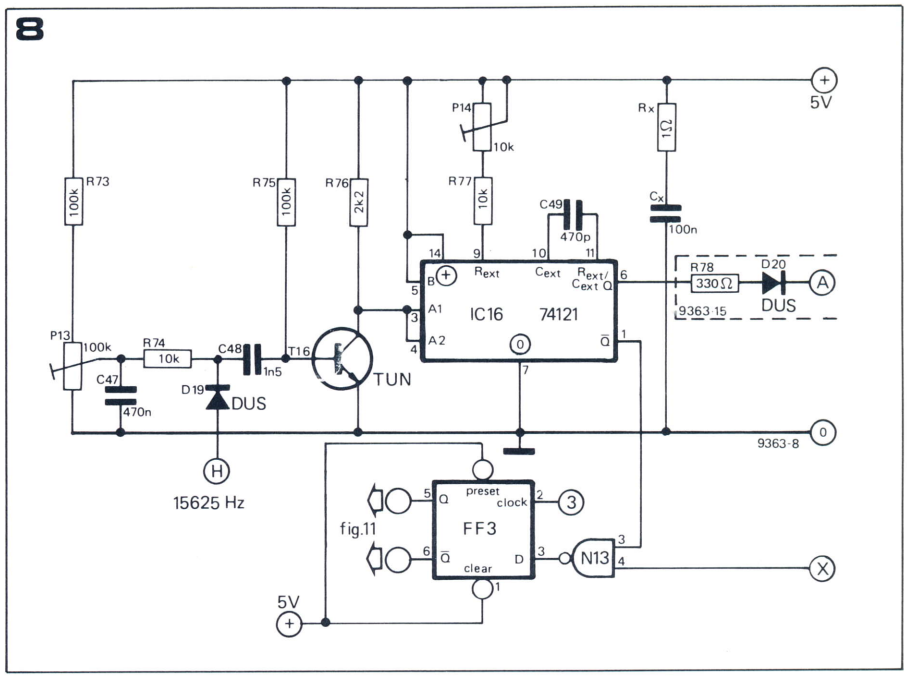
The circuit (figure 8) is almost identical to that which produces the upper and lower boundaries, but it is triggered from the line sync oscillator and produces a video pulse that overlaps the line sync pulse, thus giving a white bar at the left- and right-hand edges of the picture.

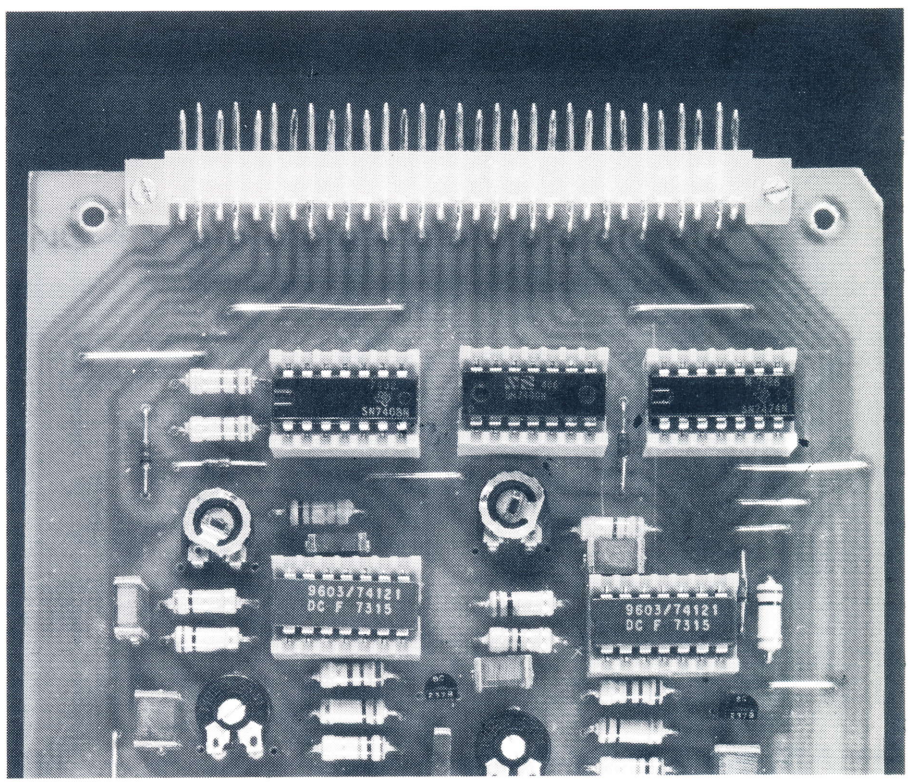
The video pulse width is about 24 μsec. and the timing diagram for this circuit is given in figure 7. P14 adjusts the pulse width, and hence the width of the vertical bars, while P13 adjusts the delay time, and hence the position of the boundaries. FF3 is used to control the sound effects unit which will be described later. Pin 2 (point 3) of FF3 is connected to pin 6 of IC1, which generates the horizontal ball signal. Within the boundaries of the court the $\overline{Q}$ output of IC16 is high, and point X is normally high, so the output of N13 holds the D input of FF3 low, and the ball signal cannot trigger it. If, however, the ball crosses the left- or right-hand boundary then the $\overline{Q}$ output of IC16 will be low, so the D input of FF3 will be high and the flip-flop can be triggered by the horizontal ball signal applied to the clock input (point 3). This means that the sound unit is activated only when the ball crosses the left- or right-hand boundary.

synchronous sound

The fun of playing the game cannot be complete without the excitement of the sound of the smash and bounce. The circuits described here will produce a variety of sounds that not only create an atmosphere of 'presence' but also give unmistakable indication when a mark is scored.

For this purpose, five different sounds are provided; the pitch and decay time of each of them can be varied according to personal taste.





Circuit Description

The circuit diagram of figure 9 shows the smash and bounce sound generators. Four generators use COS-MOS NAND gates. The fifth (T17 and T18) is a multivibrator; it is unique in that it is not connected to the power supply!

When flip-flop FF3 (see figure 8) indicates a mark scored by applying a positive step to the circuit of figure 9, it sets off a short and gradually decaying oscillation. The duration of the oscillation depends on the value chosen for C66.

The active elements of the other signal generators are COS/MOS NAND gates, four of which are housed in one IC 4011. The feedback controls (P15 . . . P18) are set so that each circuit is just on the verge of oscillation.

The sound effect will then be a damped sinusoidal oscillation with a frequency determined by the time constants of the twin-T feedback network. The duration is determined by the value of the coupling capacitors (C53, C57, C61, C65).

Different sound effects are produced for the ball being struck by the right or left

Figure 8. Circuit for producing the vertical boundaries. In this case, no modifications to the original circuit are required. The extra flip-flop will be used in conjunction with a sound effects generator to be described later.

Figure 9. Five separate sound effect generators are used. Four of these simulate the impact when the ball strikes the bats and the upper and lower boudaries, the fifth sound indicates a mark scored.

player's bat, or bouncing against the top or bottom boundary. A bat hitting the ball is accompanied by a sharp click; a bounce at the top or bottom of the field is more like a thud.

'Out' balls will retain their vertical motion and, therefore, continue to hit the upper and lower boundaries. This would cause a regular bouncing sound effect. This sound is suppressed by ANDing the Q and $\overline{Q}$ outputs of FF1 with the $\overline{Q}$ output of FF3. When the ball is 'out' the $\overline{Q}$ output of FF3 is at logic '0', blocking the AND gates.

The component values shown in the diagram are to be taken as an example; the sounds can be adapted according to taste by altering the capacitor values.

The various signals are summed and applied to an amplifier.

Football

An obvious extension of the possibilities discussed earlier is a simple football game. A field with centre line is already available. All that is required is the addition of goal posts.

These posts can be simulated in two ways, either by erecting them inside the field, or by adding a 'window' at the centre of both vertical boundaries. In the latter case the goal line coincides with the boundary, like in real soccer. Figure 10 shows the required modifications to the vertical boundaries circuit (IC16): one more mono-stable (IC21) with a trigger delay circuit is sufficient.

The position and width of the goals are set by P19 and P20 respectively. The signals that determine the vertical boundaries and the goals ($\overline{Q}$ of IC21) are applied to the video modulator via an AND gate and a diode.

The ball must now rebound from the remaining field boundaries only and not from the goals. To achieve this, the $\overline{Q}$ output of FF2 is connected to its D input. This flip-flop, which determines the horizontal direction of the ball movement will now change state at every clock pulse.

The most convenient way to acquire the clock pulse for FF2 is to AND the ball signal and the vertical boundary signal. The combined signal could be applied to the clock input of FF2. The flip-flop will then receive clock pulses at line frequency during the period that the ball coincides with the white part of a vertical boundary. If the ball goes into the goal, no clock pulses will arrive at the flip-flop. The direction of the horizontal ball movement will remain unchanged, causing the ball to leave the picture. Goal!

There is, however, one drawback to this method: if the ball has not bounced back out of the white field boundary before the next clock pulse arrives, the direction of the ball movement will change again causing the ball to reverse indefinitely and fail to re-enter the field.

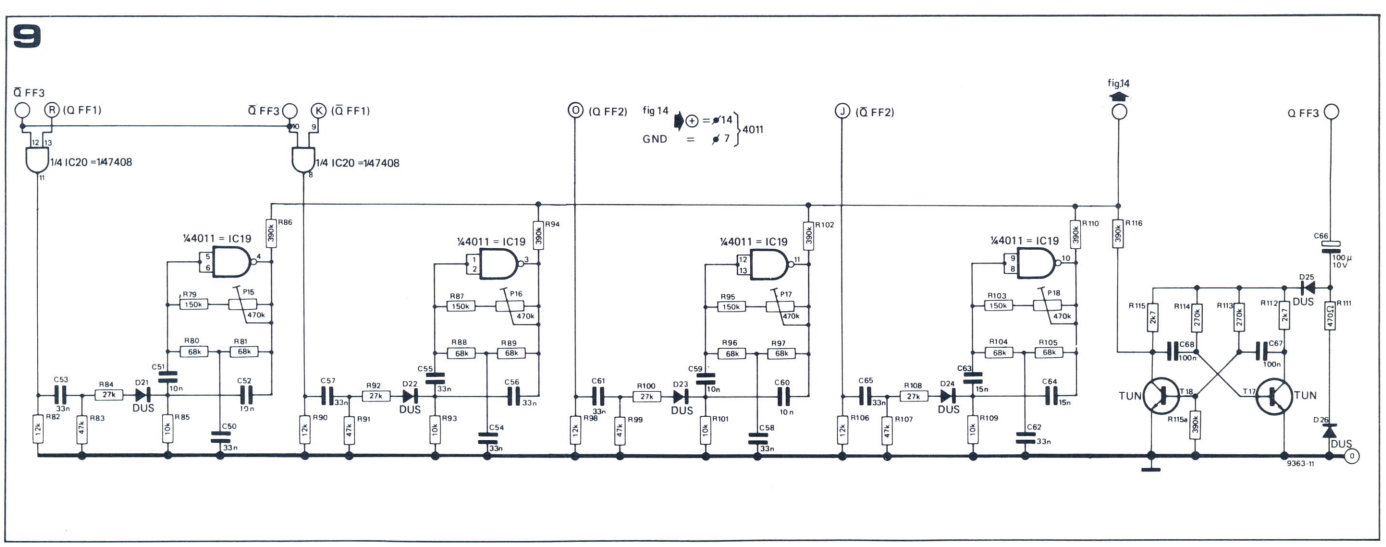
An additional flip-flop (FF4) is used to prevent this. Its D input is connected to the vertical boundary signal; the clock input is connected to the ball signal. The logic state at the Q output of this flip-flop can only change when the flip-flop is 'clocked' by the ball signal. The Q output then assumes the logic state at the D input – determined by the boundary signal. The Q output will not change as long as the ball and boundary signals coincide – irrespective of the number of clock pulses. This means that the Q output will change state once when the ball hits the boundary. This signal can be used to clock FF2.

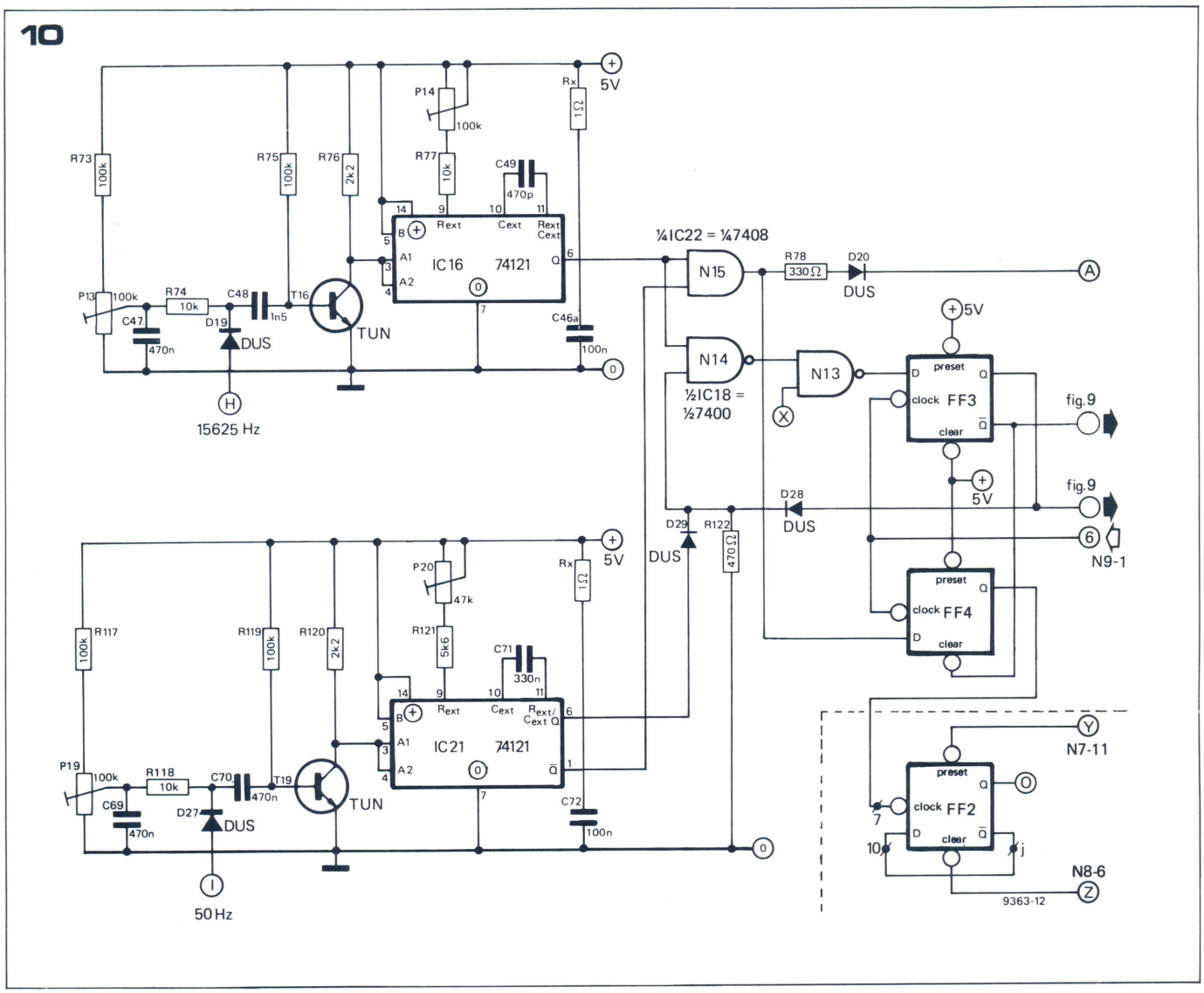
Adding FF4 is a major improvement, but it is not yet sufficient to guarantee reliable operation. The ball can leave the field through the goal, but it still moves up and down. This means that the ball, even though off the field, will hit the goal posts. As soon as it hits the edge of the boundary, above or below the goal, FF4 will clock FF2 causing the ball to re-enter the field. To prevent this, the 'clear' input of FF4 is connected to the Q output of FF3. This will block the clock pulses to FF2 after a goal has been scored. FF3 is already part of the sound circuit (indicating a goal).

The Q output of FF3 must only become logic '1' when the ball enters the goal. Moreover, this output condition must be maintained as long as the ball is 'out'. Starting from the situation when the ball is within the field area and the Q output of FF3 is logic '0', the operation of this section of the circuit can be explained as follows.

Inside the goal, the Q outputs of both IC16 and IC21 are '1'. The N14 output is, therefore, '0' and the D input of FF3 is '1'. As soon as the ball enters the goal, the clock pulses applied to FF3 coincide with this logic '1' condition at the D input. The Q output then becomes logic '1'. Since this output is connected to the D29/D28 OR gate, a '1' is applied to one of the inputs of N14.

The possibility of FF3 changing state is now determined by the vertical field boundary (IC16) and the ball position only. As long as the ball is 'out' the output state of FF3 will not change. When one of the 'serve' buttons is pushed the ball will re-enter the field and the Q output of FF3 will change back to logic '0'. The flip-flop should not become '0' immediately, as otherwise an unwanted 'goal' sound could be generated. This could happen when the ball is served by the opponent, so that it has to cross the field rapidly to 'appear' from the other side. To prevent this, one of the inputs of N13 is connected to point X, which is at zero voltage as long as one of the start switches is depressed. This will





only work properly if contact X makes before (or simultaneously with) contacts Y and Z. If this is not the case an unwanted 'goal' sound will be heard when serving; points Y or Z must then be used instead of point X.

Hole-in-the-net

As far as we know, this is an entirely new game. A more simple version does exist, where one player has to send the ball through a 'hole in the wall'.

The 'hole in the net' game is rather more complicated. The field and the horizontal position of the players are the same as in the tennis game. However, it is impossible to play normal tennis because the ball bounces back off the 'net'.

There are three ways to get the ball into the opponent's side of the field. The first two are holes in the net, one corresponding to each bat. As each player moves his or her bat up and down, the corresponding hole in the net moves up and down with it. The trick is to hit the ball and then quickly place the hole in the path of the ball.

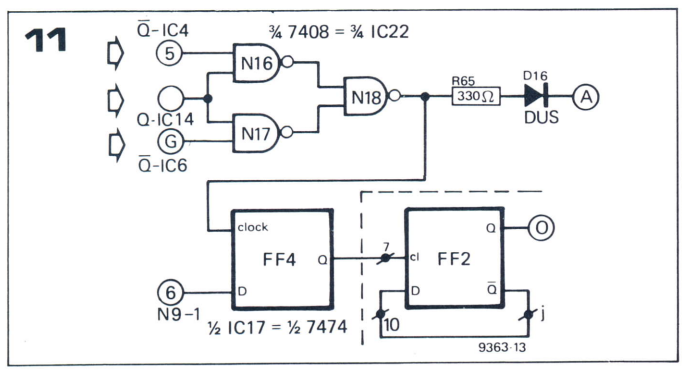
The third possibility to get the ball across is sheer luck . . . If the ball hits the net at precisely the right moment, the flip-flop that determines the direction of the horizontal ball movement may receive two clock pulses. The ball will then change direction twice, with the 'net' result that it flies straight over the centre line.

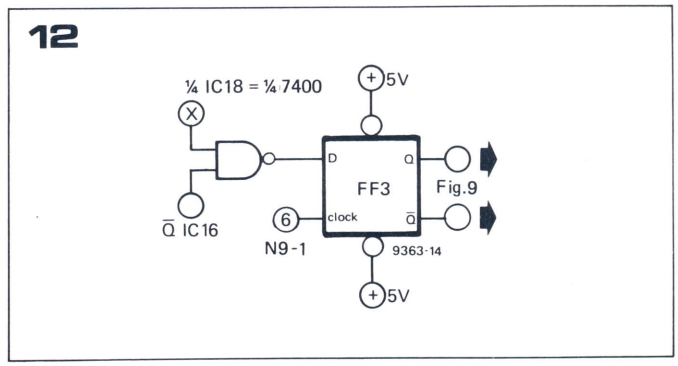
Obviously this game is more difficult than an ordinary tennis game, since one must not only hit the ball but also position the hole in the net correctly. A novice at the game will quite often send the ball into his own goal.

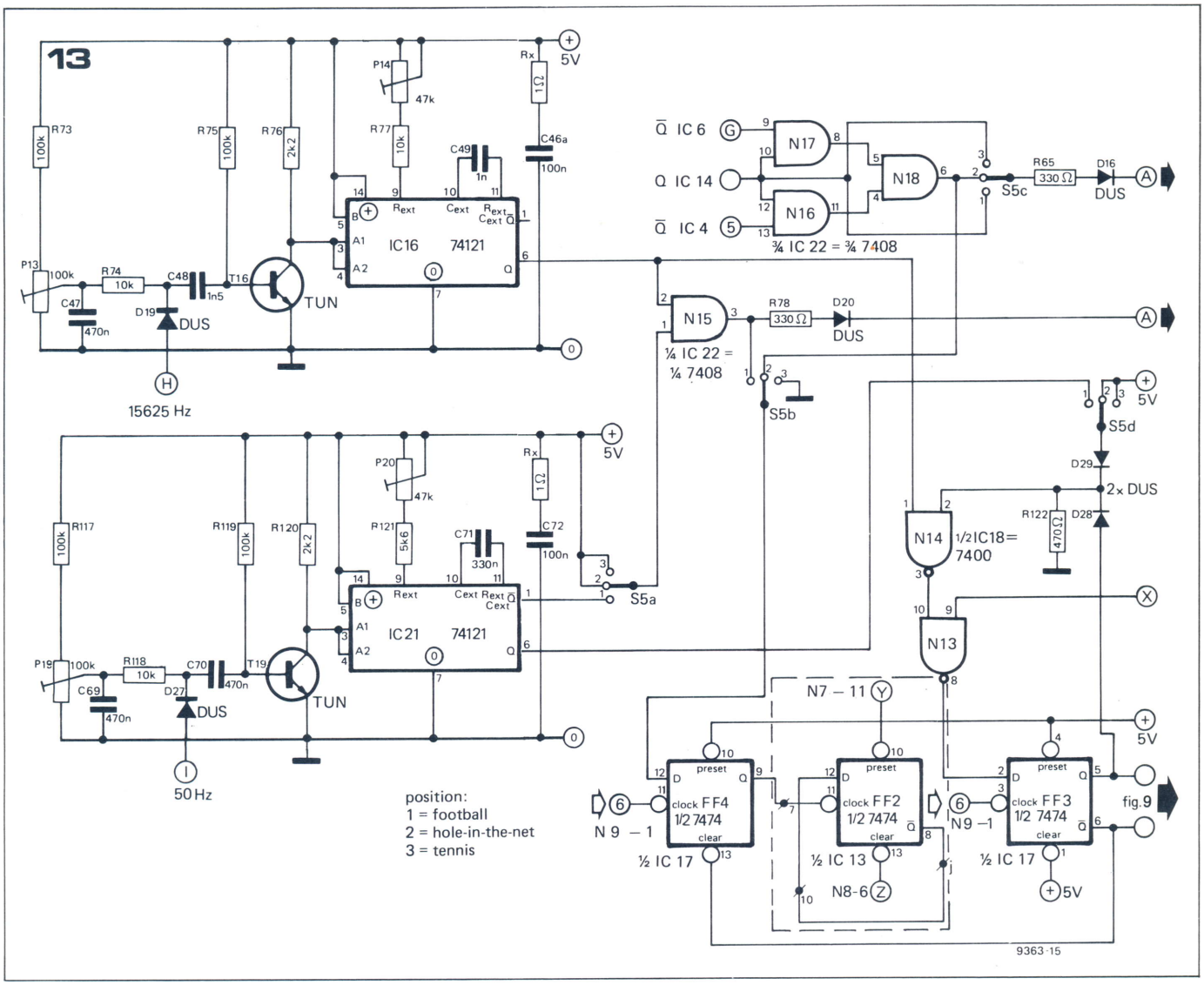
Adding this extension to the original game requires only very few modifications (see figure 11).

Three gates are added to the centre line ('net') generator. These gates use the vertical 'bat' signal to blank the video signal for the centre line. As a result, the vertical position and the size of the holes correspond exactly to those of the bats.

An additional flip-flop is required to bounce the ball back off the net. The circuit is similar to that used in the football game for rebounding from the







vertical boundaries. FF4 can be used for both circuits, provided one or two switches are added.

There is no gap in the vertical boundaries ('goal') for this game, so a mark is scored when the ball crosses a vertical boundary at any point – as in the tennis game. The same sound effects circuit can therefore be used for both games (figure 12).

Combining the three games

The diagram of figure 13 shows that it is relatively simple to design a combined circuit suitable for all three games: TV tennis, football and hole-in-the-net. For clarity's sake only those sections of the circuit are shown where modifications are to be carried out. The letters at the various connection points refer to the interface with the original TV tennis circuit.

In the new circuits, 1 Ω resistors (Rx) are included in series with the decoupling capacitors for the integrated circuits. It is recommended to add these resistors to the basic circuit as well; they will improve picture quality.

The amplifier

The amplifier design shown in figure 14 is quite straightforward but adequate for the purpose. The signals from the sound effects generators (figure 9) are

Figure 10. Additional circuit for 'football'. Part of the vertical boundary is blanked to simulate the goal.

Figure 11. Holes in the net are simulated by partial blanking of the centre line. This only requires a minor addition to the circuit for the centre line.

Figure 12. Circuit addition to control a sound effect generator.

Figure 13. Combination of the additional circuits for hole-in-the-net and football requires a selector switch.

Figure 14. The audio amplifier is quite straightforward.

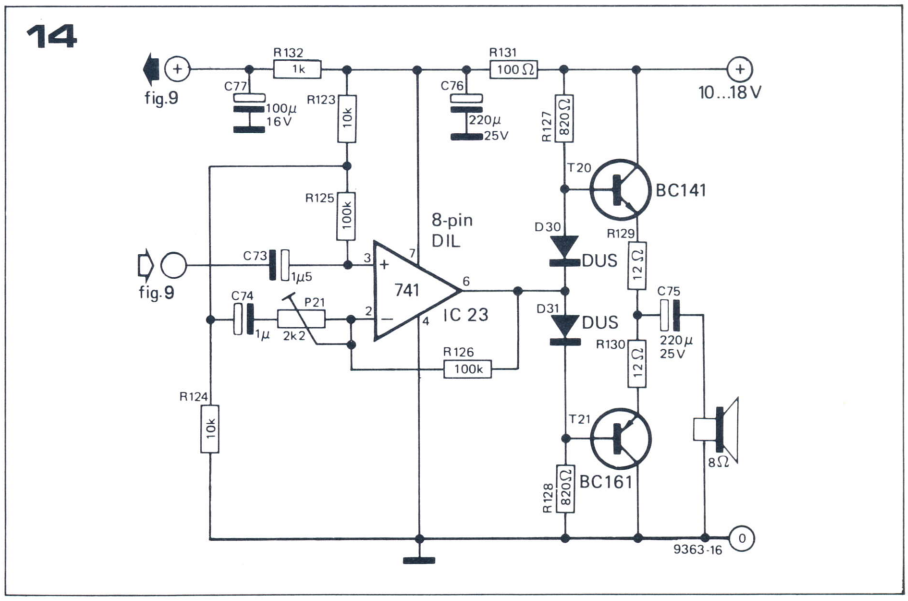


Figure 15. The p.c. board and component layout for all additional circuitry, i.e. the combination of figures 4, 6, 9, 13 and 14. (EPS 9363).

Missing link

We regret that there are a few errors in the component layout shown in figure 15.
'R115' between R113 and R116 should be R115A; 'R94' between R98 and R101 should be R99; 'C44' between IC16 and R77 should be C49; 'T20' between IC21 and C70 should be T19.

amplified to the comfortable level of about 750 milliwatts.
The volume control (P21) can be a preset. When setting this control, take care that the amplifier is not overloaded; this is quite audible, the sounds develop a nasty twang.

The p.c. board

Combination of the circuits shown in figures 4, 6, 9, 13 and 14 gives the total extension circuit. The printed circuit board for these additions is the same size as the p.c. board for the basic game, so that it can be mounted on top of the latter. All connections are at one end of the board, so that it can easily be hinged up should final adjustments to the basic board be required. The wiring between the two boards should not be neatly bundled; it is better to run the wires criss-cross to reduce crosstalk.

Final adjustments

Few problems are likely to arise if the basic equipment has been correctly set up.
With S5 switched to 'TV tennis', the centre line is positioned by adjusting P10.
The next step is the positioning of the horizontal boundary. P12 is used to set the width, P11 to set the position. The vertical boundary can then be adjusted in the same way, using P14 and P13 for width and position respectively.
Having carried out these adjustments, switch S5 to 'hole-in-the-net'. Two holes should appear in the centre line, one corresponding to the vertical position of each bat. There is no adjustment for this, so if it does not work there must be a mistake in the wiring . . .
The last video adjustment is the correct positioning of the goals for 'football'. Switch S5 to 'football'; the height and position of the goals is set by P20 and P19 respectively. Finally the sound effects units must be adjusted. All NAND generators must be set on the verge of oscillation, by means of P15 . . . P18.
The gain of IC23 is set with P21 to a comfortable level, where there is no audible distortion. ◀

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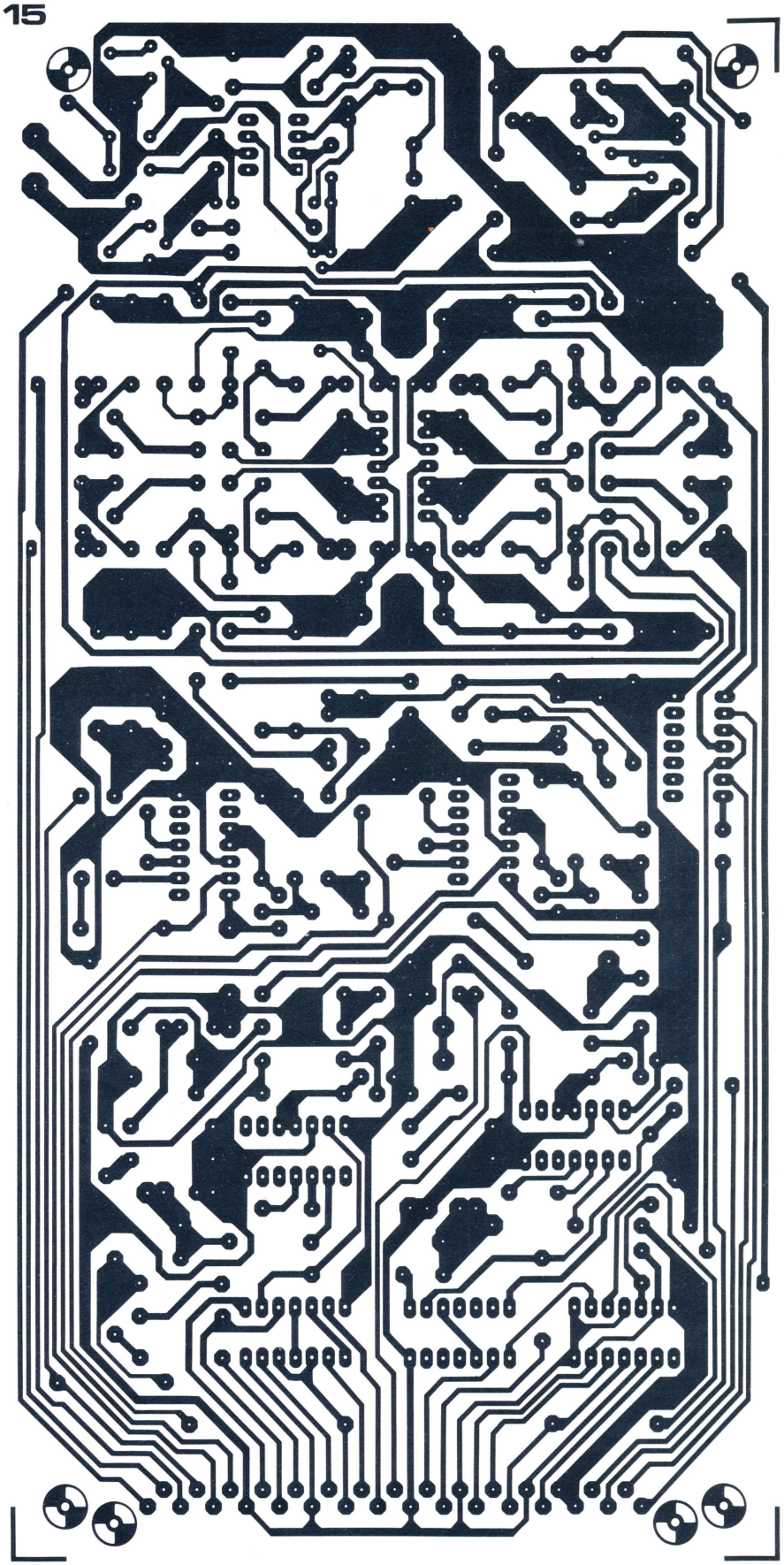

Parts list to figures 4, 6, 9, 13, 14 and 15

Resistors:

Figure 4:

R60,R62 = 100 k
R61,R64 = 10 k
R63 = 2k2
R65 = 330 Ω
P10 = 100 k (preset)

Figure 6:

R66,R68 = 100 k
R67 = 10 k
R69 = 2k2
R70 = 4k7
R71 = 330 Ω
R72 = 470 Ω

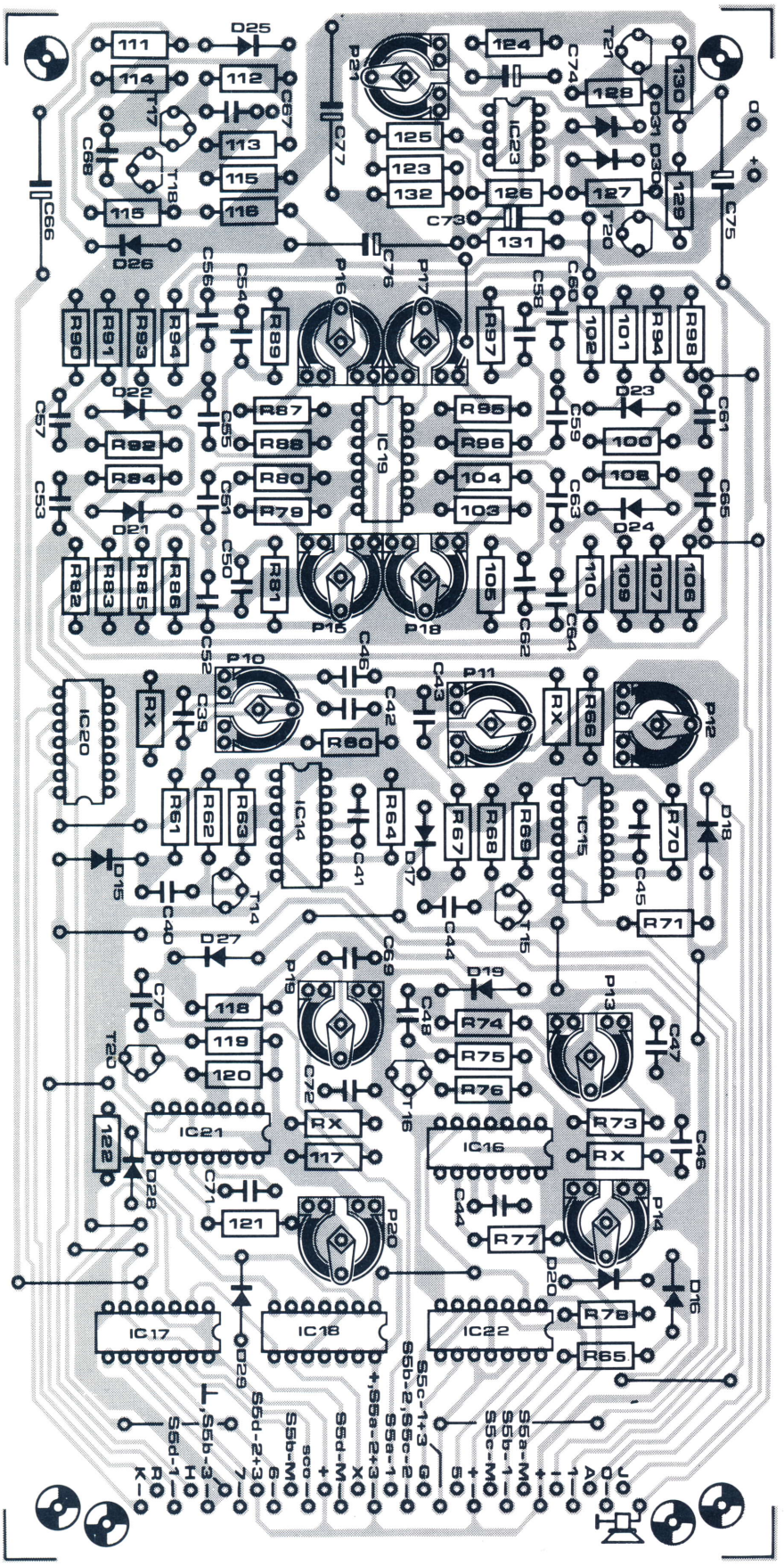

Figure 9:

R79,R87,R95,R103 = 150 k
R80,R81,R88,R89,R96,R97,R104,
R105 = 68 k
R82,R90,R98,R106 = 12 k
R83,R91,R99,R107 = 47 k
R84,R92,R100,R108 = 27 k
R85,R93,R101,R109 = 10 k
R86,R94,R102,R110,R115a,
R116 = 390 k
R111 = 470 Ω
R112,R115 = 2k7
R113,R114 = 270 k
P11 = 100 k
P12 = 22 k
P15 . . . P18 = 470 k (preset)

Figure 13:

R73,R75,R117,R119 = 100 k
R74,R77,R118 = 10 k
R76,R120 = 2k2
R78 = 330 Ω
R121 = 5k6
R122 = 470 Ω
P13,P19 = 100 k
P14,P20 = 47 k

Figure 14:

R123,R124 = 10 k
R125,R126 = 100 k
R127,R128 = 820 Ω
R129,R130 = 12 Ω
R131 = 100 Ω
R132 = 1 k
P21 = 2k2
R_X = 1 Ω (4x)

Capacitors:

Figure 4:
C39 = 470 n
C40 = 1n5
C41 = 82 p
C42 = 100 n

Figure 6:
C43,C44 = 470 n
C45 = 820 n
C46 = 100 n

Figure 9:
C50,C53 . . . C58,C61,C62,C65 = 33 n
C51,C52,C59,C60 = 10 n
C63,C64 = 15 n
C66 = 100 µ/10 V
C67,C68 = 100 n

Figure 13:
C46a,C72 = 100 n
C47,C69,C70 = 470 n
C48 = 1n5
C49 = 1 n

Figure 14:
C73 = 1µ5/16 V
C74 = 1 µ
C75 = 220 µ/25 V
C76 = 220 µ/16 V
C77 = 100 µ/16 V

Semiconductors:

Figure 4:
D15,D16 = DUS
T14 = TUN
IC14 = 74121

Figure 6:
D17,D18 = DUS
T15 = TUN
IC15 = 74121

Figure 9:
D21 . . . D26 = DUS
T17,T18 = TUN
IC19 = 4011
IC20 = 7408

Figure 13:
D19,D20,D27,D28 = DUS
T16,T19 = TUN
IC16,IC21 = 74121
IC17 = 7474
IC18 = 7400
IC22 = 7408

Figure 14:
D29,D30 = DUS
T20 = BC141
T21 = BC161
IC23 = 741

Mechanical parts:

Figure 13:
S5 = rotary switch, 4-pole 3-way

W.G. Paans

calendar

Many mechanical and electro-mechanical clocks and watches are now provided with date indication. Addition of a calendar to an electronic digital clock is a fairly simple matter, and the circuit given here gives the month as well as the date.

As the calendar is an addition to a digital clock a control signal must be derived from the clock to change the date. This can be derived from the changeover from 23.59 to 00.00 with a 24-hour clock, or if used with a 12-hour clock the changeover from 11.59 to 12.00 may be used. However, since this occurs every 12 hours a ÷ 2 flip-flop must be inserted between clock and calendar to give a pulse once every 24 hours.

Like all the best calendars, this calendar knows whether the last day of the month falls on the 28th (February), the 30th or the 31st. Those who are worried about the 29th of February can add the optional leap-year correction circuit, in which case the calendar will not need to be reset until the year 2100, when a century correction (omission of leap-year) becomes necessary.

The calendar is simply a logical extension of the hours, minutes and seconds counters in the clock, but counting days and months instead. The resetting functions are, of course, considerably more complicated due to the differing number of days in each month. Since the year begins with the first month, and each month begins with the first day, it is not possible to use simple decade counters such as the 7490, which can be reset to zero. Instead, presettable counters must be used, so that they can be preset to one at the beginning of the year or month. A suitable choice is the 74163, which is a four-bit binary counter with synchronous preset and clear. Two of these counters make up the days and tens of days counter, and as the capacity of the 74163 is 4 bits, one of these IC's will suffice for the

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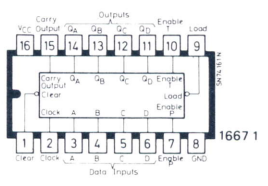

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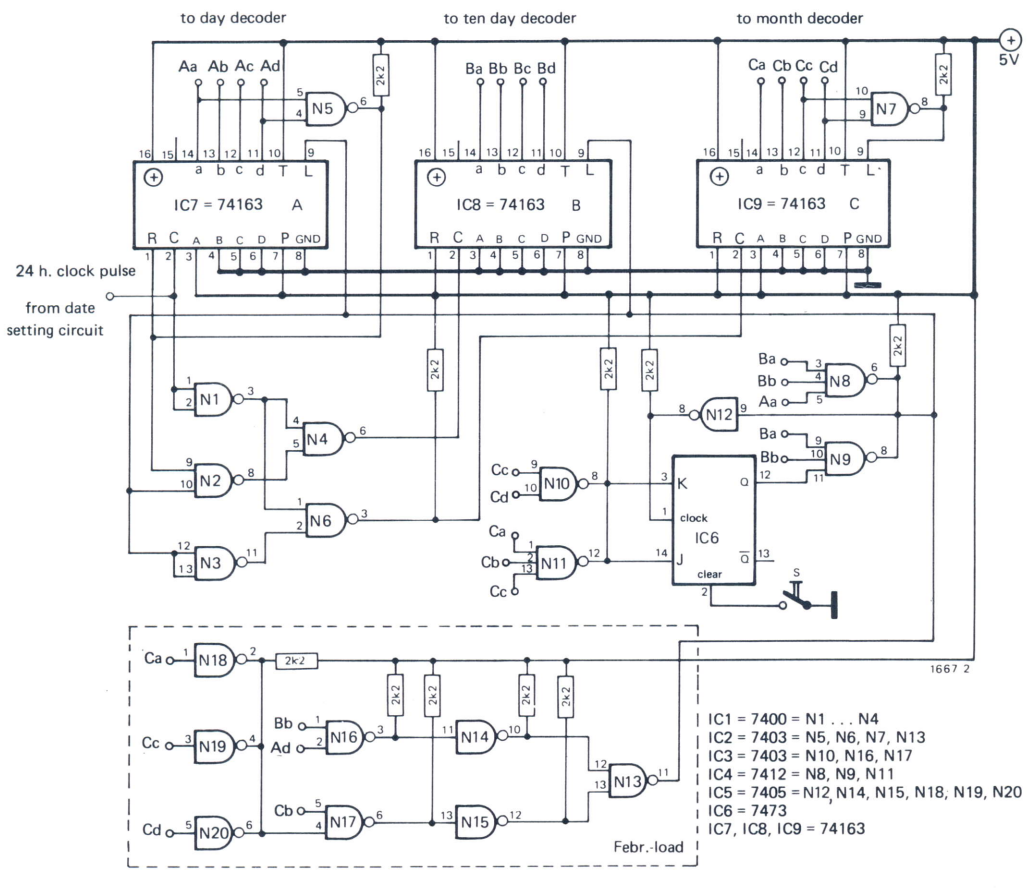


months counter. The pin configuration of the 74163 is given in figure 1. Points to watch with this IC are:

i) unlike the 7490 it counts on a positive-going edge of the input waveform.

ii) for resetting purposes a logic '0' is required.

iii) counting may only take place when there is a '1' at both the enable inputs P and T.

iv) when there is a '0' at the load input the count function is inhibited. The next positive-going transition of the clock input transfers information from the data inputs to the outputs.

Counter Circuit

The circuit of the counter section of the calendar is given in figure 2. IC7 counts the days, IC8 counts tens of days and IC9 counts months. The enable inputs of all three counters are permanently connected to positive supply, as are the clear inputs of IC8 and IC9. The data inputs of the three counters must have the correct presetting data hardwired into them. The day counter is preset to 1 at the beginning of each month, so the A input is connected to positive supply and the B, C and D inputs to ground. The tens of days counter is preset to zero so all the data inputs are grounded. The month counter is preset to 1, like the day counter.

IC7 receives one pulse every 24 hours from the digital clock at pin 2 (clock input). This IC is connected so that it normally counts up to 9 before resetting to zero. When the count reaches 9 (binary 1001) the a and d outputs of the counter are high, so the output goes low, taking the synchronous clear input (pin 1) to '0'. On the tenth clock pulse the counter is reset synchronously to zero. This sequence is of course interrupted when the counter is preset to 1 at the beginning of each month.

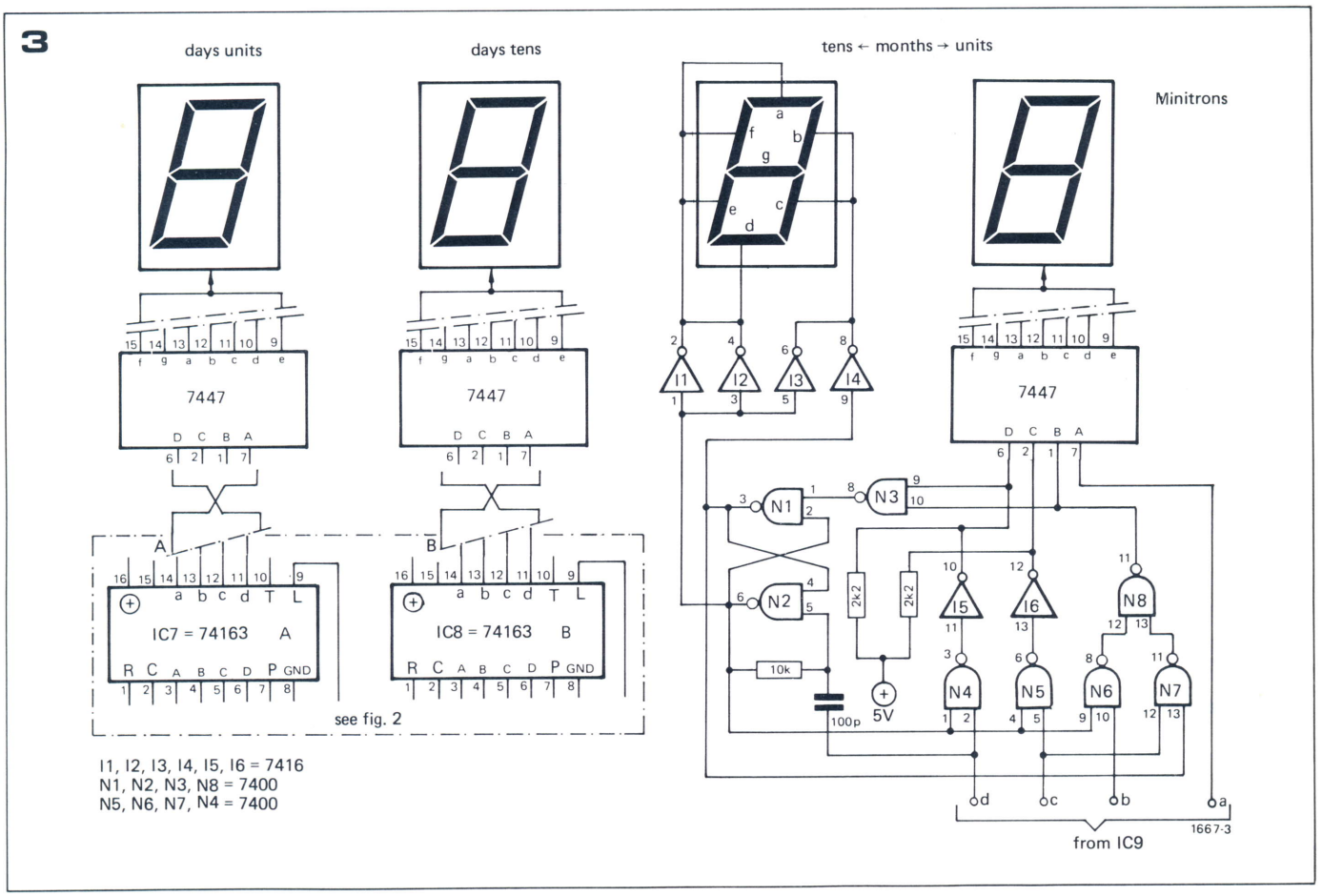
While the output of N5 is low this also holds pin 9 of N2 low, so its output is high. The tenth clock pulse which resets IC7 can therefore pass through N1 and N4 to the clock input of IC8. IC8 therefore counts once every ten clock pulses. As stated earlier IC7 and IC8 must be preset at the beginning of each month, the count that they reach before this occurs depending on the number of days in the preceding month. It is evident from table 1 that with two exceptions the number of days in the month alternates between 31 and 30. The exceptions are February, which has 28 days, August, which has 31 days after July's 31 and December/January similarly. It is thus possible to indicate the number of days required in each month with a flip-flop whose state is changed each month, the only corrections necessary being a) additional circuitry to detect when the month is February, and b) circuitry to inhibit the changeover of the flip-flop at the July/August and December/January transitions. The flip-flop is IC6, and the 'February detection circuit' is contained in the dotted box. This part of the circuit operates as follows: Assume that the next transition is from a month with 30 days to one with 31 days (say April/May). The Q output of IC6 will initially be high. When the count of IC7 and IC8 reaches 30, outputs Ba and Bb of IC8 will go high. This means that all three inputs of N9 are now high so the output is low, taking the load inputs of IC7 and IC8 to '0'. On the next clock pulse IC7 and IC8 are thus preset. The output of N9 also holds the input of N3 low. The output of N3 is thus high, so the clock pulse is allowed through N6 to the clock input of IC9. Immediately IC7 and IC8 are preset the output of N9 goes high again. The output of N12 thus goes low. This is connected to the clock input of IC6 so the flip-flop changes state and the Q output goes low.

At the end of the next month, since the Q output of IC6 is low the output of N9 must remain high and the transition cannot take place on day 30. Instead N8 takes over, and on day 31, when outputs Ba and Bb and output Aa are all '1', then the output of N8 goes low and the sequence repeats. Inhibition of the

Figure 1. Pin configuration of the 74163 used in this design.

Figure 2. Basic circuit of the counting section of the calendar.

Figures 3 and 4. Two alternative decoding circuits for the calendar.



flip-flop changeover during the July/August transition is accomplished by N11. As July is the 7th month (binary 0111) outputs Ca, Cb, and Cc are connected to the inputs of N11. When these are all '1' (during July) the output of N11 is low. This takes the J and K inputs of IC6 low, inhibiting the change of state. N10 performs a similar function during the December/January transition.

The 'February detection circuit' operates as follows: the rather complicated looking array of gates performs the logic function:

'February transition' =

$$Cb \cdot \overline{Ca} \cdot \overline{Cc} \cdot \overline{Cd} \cdot Bb \cdot Ad.$$

Which is to say that the output of N13 goes low when the month is February (binary 0010) and the day is 28 (Ad = 1, Bb = 1).

The only point left to explain in figure 2 is the presetting of the month counter. This is allowed to count up to 12. When the count reaches 12 outputs Cc and Cd are high so the output of N7 holds the load input low. On the next clock pulse the counter is synchronously preset to 1.

Display Decoding

To provide an intelligible display the outputs of the three counters must, of course, be decoded. Two alternative decoding circuits are given, and the choice is up to the constructor. Since the day counters have BCD outputs these are easily decoded, in both figures 3 and 4, using 7447 BCD/seven-segment decoder-drivers. Although the circuits shown use Minitron displays, LED displays may equally well be used (with appropriate segment series resistors).

As the month counter counts to 12 in straight binary decoding is a little more difficult. The month decoding of figure 3 operates as follows:

when the month count is less than 10 the flip-flop comprising N1/N2 is reset and the output of N1 is low. This means that the data from IC9 (connected to inputs a, b, c, d) is allowed through N4/I5, N5/I6 and N6/N8 (data on input a is connected direct to decoder) and is decoded into the months (units) display.

The inputs of I_1, I_2 and I_3 are all connected to the output of N2, which is high, so their outputs are low and the ten month display is '0'. If a leading zero is not required on the ten month display then these inverters may be omitted. When the month count reaches 10 (binary 1010) the output of N3 goes low, setting flip-flop N1/N2. The outputs of I_1, I_2 and I_3 are now high, while the output of I_4 is low, so the ten month display is 1.

The low output of N2 inhibits the data on the b, c and d inputs from passing through N4, N5 and N6. The high output of N1 allows the data on the c input through N7. During months 10 to 12 therefore inputs C and D of the 7447 are low, the B input receives data from the c output of the counter, while the A input continues to receive 'a' data. During month 10 (binary 1010) the 7447 receives input code 0000 and thus the display is 0. During month 11 (binary 1011) the input of the 7447 is 0001 (display 1) and during month 12 (binary 1100) the input code is 0010 and the display 2. During this period the ten month display is, of course, always 1. At the end of the year, when the month counter is preset back to 1, the d input to the decoder goes low. This transition is differentiated by the 10 k and 100 p on the input of N2, producing a short negative-going pulse that resets the flip-flop.

Month	Number of days	IC6 Q outputs	IC6 J and K inputs
January	31	0	1
February	28	1	1
March	31	0	1
April	30	1	1
May	31	0	1
June	30	1	1
July	31	0	0
August	31	0	1
September	30	1	1
October	31	0	1
November	30	1	1
December	31	0	0

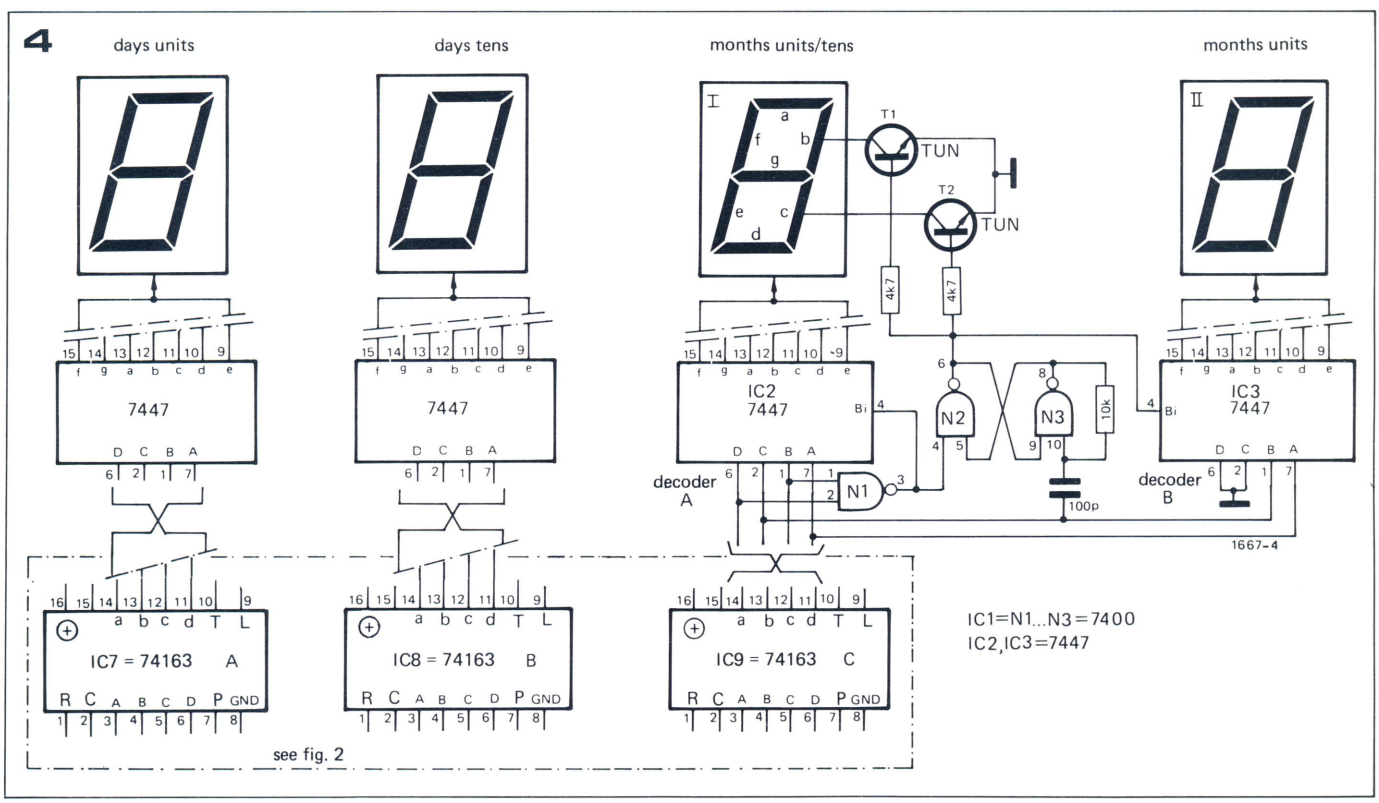
Table 1. Number of days in each month and the corresponding states of flip-flop IC6.

Figure 5. Date setting circuit.

Figure 6. Showing the addition of automatic leap-year correction to the calendar.

The month decoding of figure 4 operates on a somewhat different principle. Basically, for counts of less than 10 the months units are decoded by IC2. For counts from 10 to 12 the months units decoding is transferred from IC2 to IC3, while IC2 counts the tens of months. The circuit operates as follows: for month counts below 10 flip-flop N2/N3 is reset, so the output of N2 is low. T1 and T2 are turned off and IC3 is inhibited by a '0' on the blanking input (pin 4). IC2 thus decodes the data from the output of the month counter.

When month 10 is reached the output of N1 goes low, setting the flip-flop and blanking IC2. The display is now driven by T1 and T2, which are turned on, causing a 1 to be displayed. The low state on the blanking input of IC3 is removed, and this decoder receives data on its A and B inputs from the a and c outputs of the counter. Thus for months 10, 11 and 12 IC3 receives inputs 0000, 0001 and 0010 respectively.



At the beginning of the new year the flip-flop is reset in a similar fashion to that of figure 3.

Date Setting

This is accomplished by the circuit of figure 5. With S1, S2 and S3 in the position shown the three flip-flops comprising N4-N9 are reset. The outputs of N4, N6 and N8 are thus high. One of the inputs of N3 is held low by N5 so its output is high, and both inputs of N11 are low, so its output is high. Two of the inputs of N10 are high so the 24-hour pulses connected to the other input can pass through N10 and N12 to the day counter.

If S1 is now changed over flip-flop N4/N5 is set blocking the 24-hour pulses through N10 and allowing a fast pulse train from the astable multivibrator N1/N2 through N3 and N12. This can be used for fast setting of the calendar to some value near the required date. If S1 is now reset to its original position and S2 is changed over N10 is again blocked by a '0' on pin 2. Pin 9 of N11 is now high, so the calendar may be advanced slowly to the correct date by single pulses through N11, produced by alternately setting and resetting flip-flop N8/N9 with S3. Flip-flop IC6 must, of course, be set to the correct state for the month, according to table 1.

In the 'versatile digital clock', a suitable 24 hour pulse is available at pin 8 of IC1 (FF2).

Leap Year Correction

The automatic leap-year correction is extremely simple, and consists basically of a divide-by-four counter that counts the years and gives February an extra day every fourth year. The addition of the leap-year correction to the calendar circuit is shown in figure 6. The counter consists of two JK flip-flops (IC10). Once a year this counter receives a pulse from output d of the month counter IC9. Normally at least one of the $\overline{Q}$ outputs of IC10 will be low and the base of T1 will be held down via one of the two diodes connected to these outputs. T1 will thus be turned off. During the fourth year both these outputs are high, removing the constraint on the base of T1. T1 is now turned on and off on alternate days by N21, whose input is connected to output a of IC7. On odd days T1 is off, and on even days T1 is on, holding pin 12 of N13 low. When the 28th of February arrives the 'February detection circuit' will try to operate, but since it is an even day T1 is turned on and the output of N13 remains high. It will not go low until T1 turns off on the 29th, and on the next clock pulse the day counters are preset.

Conclusion

These circuits should enable the constructor to add a calendar to most digital clocks. The construction and type of displays used are left to the reader's individual preference, and presumably will be chosen to match the existing clock.

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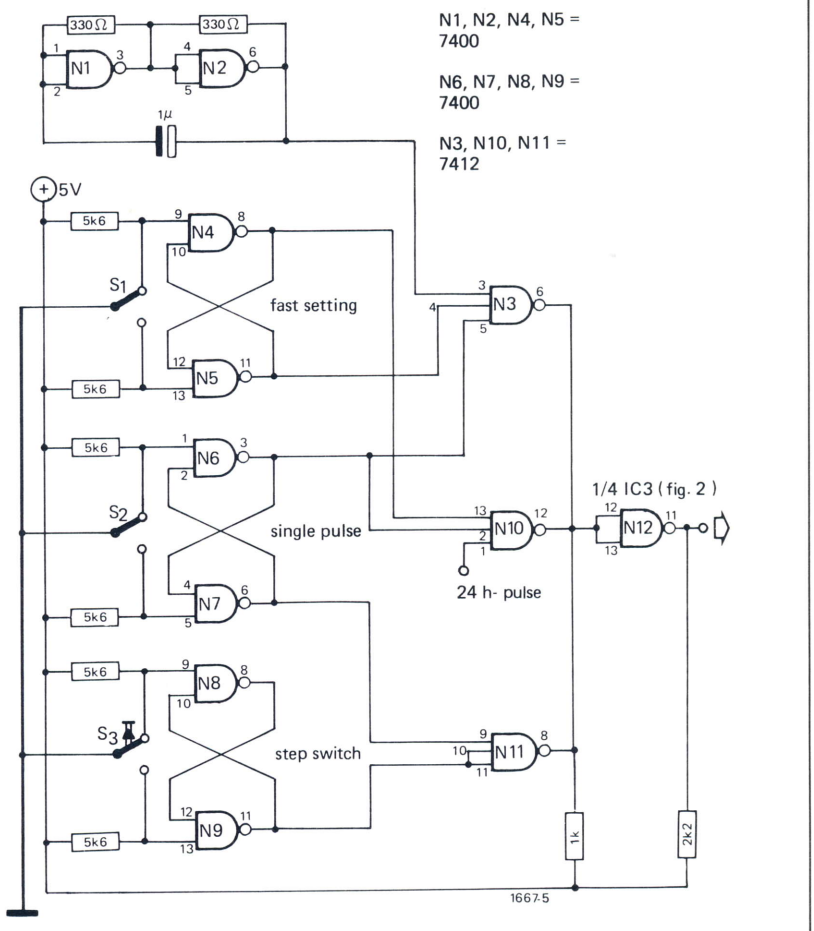

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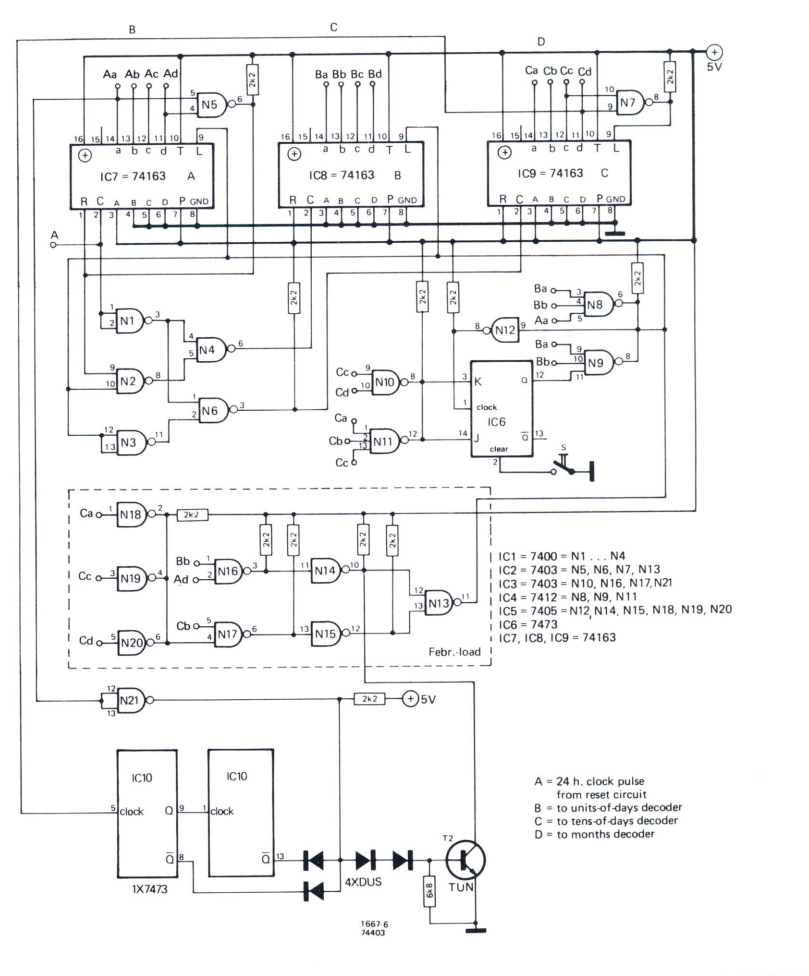


compressor

Compressors are now being used on an ever-increasing scale. They may be found in tape recorders, intercom systems and baby alarms, public address systems, discotheques and of course broadcast transmitters. A compressor supplements a manual volume control and allows a system to adjust itself to a wide range of input signals with little distortion.
The design described here should find a wide range of applications with the electronics enthusiast.

The aim of compression

Where signals with a wide dynamic range have to be processed it is desirable that as little distortion as possible should occur. The designer of, say, a public address system may have given much thought to achieving a good distortion figure, but this is of no avail if the system is overloaded by an enthusiastic speaker shouting into the microphone. It is of course possible to prevent a circuit from being overloaded by attenuating the input signal with a fixed or manually variable attenuator, but then in the example above the person who mumbles into his notes would certainly not be heard.
This is where a dynamic range compressor comes in. A compressor is basically an attenuator, or variable gain amplifier, which is controlled by the signal it is attenuating, either directly or by a control voltage derived from the signal. As the signal increases so does the degree of attenuation, so the compressor tries to keep the output signal constant whatever the input. This cannot be achieved in practice, but it is possible to limit the output to a narrow range over a wide range of input signals. In a p.a. system (figure 1) a compressor could be included between the microphone preamp and the normal volume control. The compressor, like death, is a great leveller.

Compressor Transfer Functions

At first sight it would seem to be an admirable aim to control the output signal amplitude with the input signal as in figure 2. This system has an overall gain of $\frac{K}{v_i}$, where K is a constant and v_i is the input voltage (for an attenuator of course the gain is less than 1).

So $V_O = \frac{v_i K}{v_i} = K.$

The output voltage is therefore constant for all input voltages. This seems admirable until one considers what happens

Figure 1. Block diagram of a p.a. system including a compressor.

Figure 2. A first approach to a transfer function for a compressor. This is doomed to failure however.

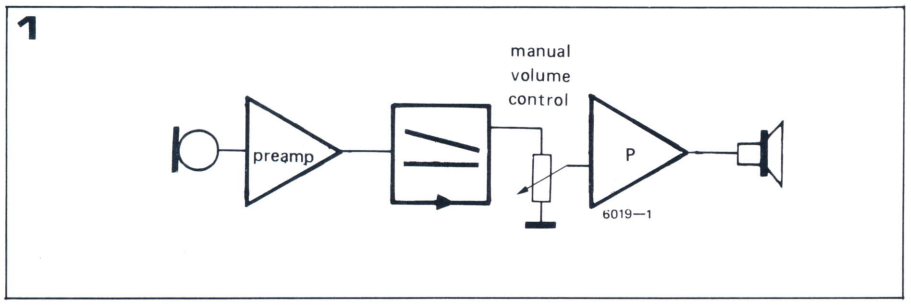
Figure 3. Black-box representation of a square-law compressor.

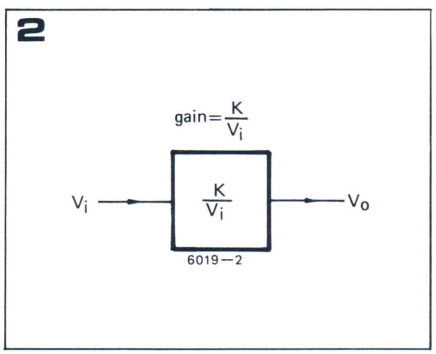
Figure 4. a. Voltage-current curve of a filament lamp. The resistance increases with increased current.
b. Compressor using a lamp and a fixed resistor.
c. Transfer function of the compressor.

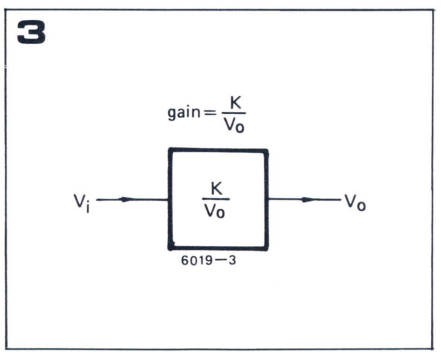
Figure 5. a. Voltage-current curve of a VDR. b. Compressor using a VDR and a fixed resistor. c. Transfer function of the compressor.

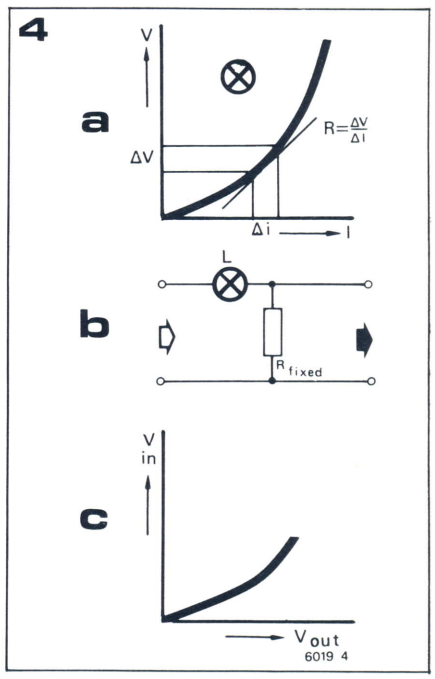
Figure 6. Dynamic characteristics of various types of compressor in response to a sudden burst of signal.

Figure 7. Block diagram of an active compressor using a peak detector to derive a control voltage which alters the attenuator.









when v_i is zero. The gain then becomes infinite and this idea becomes unnattractive.

A much better solution is to control the output signal with the output signal, which at first sight may seem odd. In figure 3 however it can be seen that the gain is $\frac{K}{v_0}$.

Therefore $v_0 = \frac{Kv_i}{v_0}$.

or $v_0^2 = Kv_i$

This is a square-law compressor function. Of course, other functions may be achieved, notably logarithmic, where $v_0 = K \log v_i$.

Practical Compressor Circuits

There are many different kinds of compressor circuit. One of the oldest and simplest circuits makes use of the non-linear resistance of an incandescent lamp, whose resistance increases as the current through the filament increases. In figure 4 the resistance of the lamp, which forms the upper limb of the attenuator, is low at low signal levels so only a small portion of the signal voltage is dropped across it. At higher signal levels the resistance increases and a larger proportion of the signal voltage is dropped across the lamp. The output signal therefore does not increase as much as it would with a normal attenuator. The thermal inertia of the lamp filament means that this circuit cannot follow the actual signal waveform but only the envelope (provided the frequency is not too low) so distortion produced by the circuit is fairly small. The thermal inertia of the filament means, however, that the circuit cannot respond quickly to sudden increases in signal, so that associated circuitry may be overloaded whilst the lamp resistance is changing. Also the range of this type of compressor is limited.

An alternative solution would seem to be the use of a voltage-dependent resistor (VDR) as in figure 5. This has a voltage versus current curve which is approximately the inverse of that of the lamp, so it is included in the lower limb of the attenuator. As the signal is increased the resistance of the VDR decreases so a smaller proportion of the signal appears across it. The response time of a VDR is quite fast so that it will follow sudden increases in signal amplitude, but unfortunately it can also follow the signal waveform so that instead of compressing the envelope amplitude whilst preserving the waveshape it simply 'rounds off' the signal peaks thus introducing distortion. Nonetheless, in certain applications where distortion can be tolerated, such as amateur radio transmitters or intercoms, it does have its uses.

It thus appears that the compressor designer is caught between two stools. A slow-acting device will cause little distortion on sustained large signals, but will not react sufficiently quickly to prevent momentary overloads of the equipment, whereas a fast-acting compressor will react in time to prevent overload, but will of itself introduce distortion. Here, however, an unusual aural phenomenon comes to the designer's aid. The ear is incapable of detecting even large amounts of distortion in transients, so that if a fast-acting compressor is applied to a sudden increase in signal it will prevent gross overloading of the system whilst the distortion it introduces will be unnoticed. Once the compressor has limited the signal, however, the ear can detect the distortion it introduces, so on sustained loud passages the slow response of the lamp-type compressor is required. In fact what is required is a compressor with a fast attack and slow decay characteristic.

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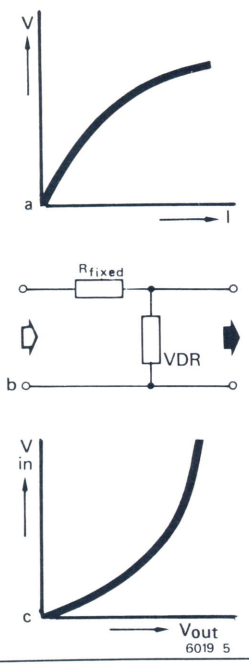

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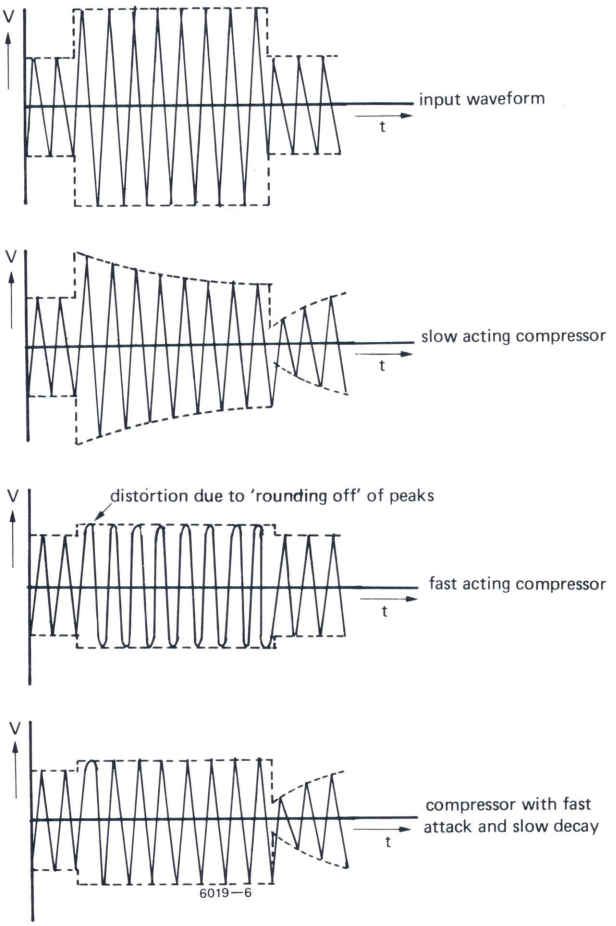

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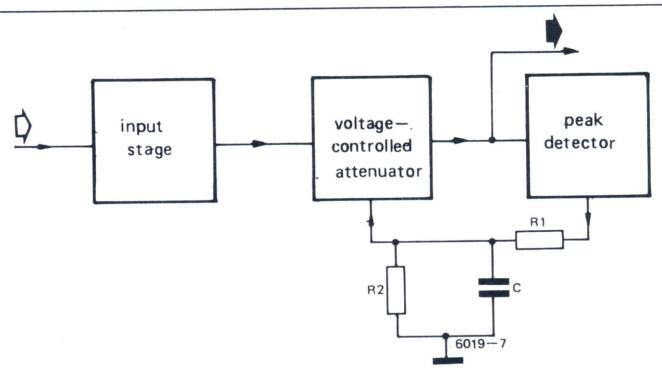

The characteristics of various types of compressor are given in figure 6. The triangular waveform was used to show how distortion is caused by a fast-acting compressor.
The discussion has so far been confined to passive devices that are controlled directly by the signal on which they operate, but for a device with different attack and decay time constants it is necessary to turn to active circuits. In figure 7 the signal passes through the input stage and into a voltage-controlled attenuator. The output voltage is taken

parts list:

resistors 1/4 Watt:
R_1, R_4, R_{10}, R_{12} = 10 k
R_2, R_9, R_{21}, R_{22} = 220 k
R_3 = 4k7
R_5 = 220 Ω
$R_6, R_{17}, R_{20}, R_{26}$ = 22 k
R_7 = 1 k
R_8, R_{15}, R_{16} = 330 k
R_{11} = 270 k
R_{13}, R_{14}, R_{25} = 3k3
R_{24} = 47 k
R_{27} = 120 k
P_1 = preset 22 k

transistors:
T_1, T_3 to T_9 = BC 109C
T_2 = BC 179C

capacitors:
C_1 = 100 n
C_2, C_{11} = 1 μ, 10 V
C_3 = 180 p
C_4 = 100 μ, 16 V
C_5, C_9, C_{10} = 560 n
C_6 = 100 μ, 4 V
C_7, C_8 = 2,2 μ, 10 V

C_{12}, C_{13} = 47 μ, 10 V
D_1 = zener diode 2,7 V
D_2 to D_5 = germanium diode matched pairs AA 119
D_6 to D_8 = silicon diode 1N914 or 1N4148

for V_b = 9 Volt: R_{18}, R_{19} = 270 Ω and R_{23} = 1k8
for V_b = 12 Volt: R_{18}, R_{19} = 330 Ω and R_{23} = 1k5

Figure 8. An LDR used in a voltage-controlled attenuator. This circuit suffers from slow response due to the inertia of the lamp and LDR.

Figure 9. An r.f. carrier type of compressor. The filter eliminates harmonic distortion of the carrier caused by the attenuator and also eliminates control-voltage noise.

Figure 10. Voltage-current curve of a diode and circuit of a simple diode attenuator.

Figure 11. Balanced type of diode attenuator eliminates control-voltage noise which appears in common mode.

Figure 12. The circuit of the final compressor design.

Figure 13. The printed circuit board and component layout of the compressor.

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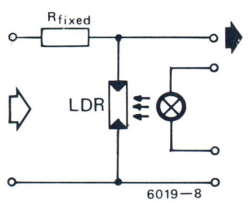

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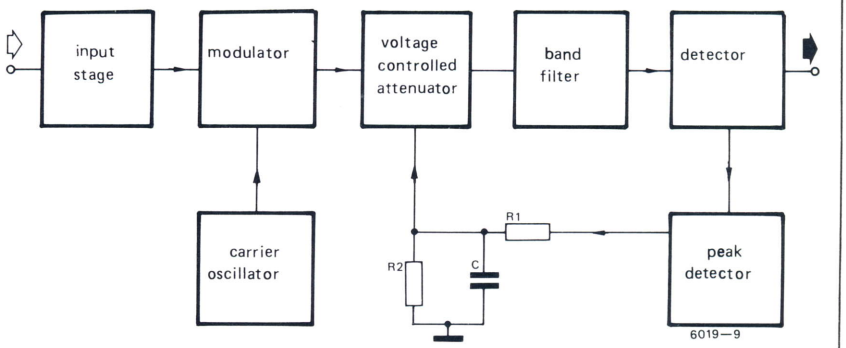

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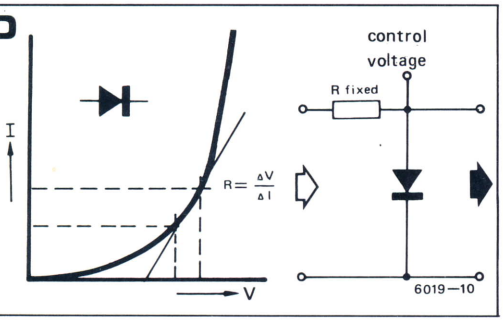

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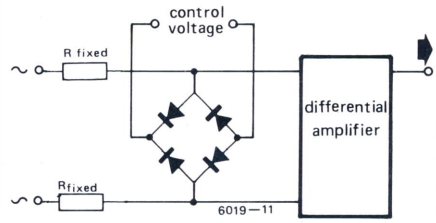

Quiescent D.C. test voltage measured with 50 k/V meter

Emitter T_1	:	2.4 V
Emitter T_2	:	8.8 V
Collector T_2	:	5 V
Collector T_3	:	5.5 V
Emitter T_3	:	3.3 V
Collector T_4 and T_5	:	6 V
Collector T_6	:	2 V

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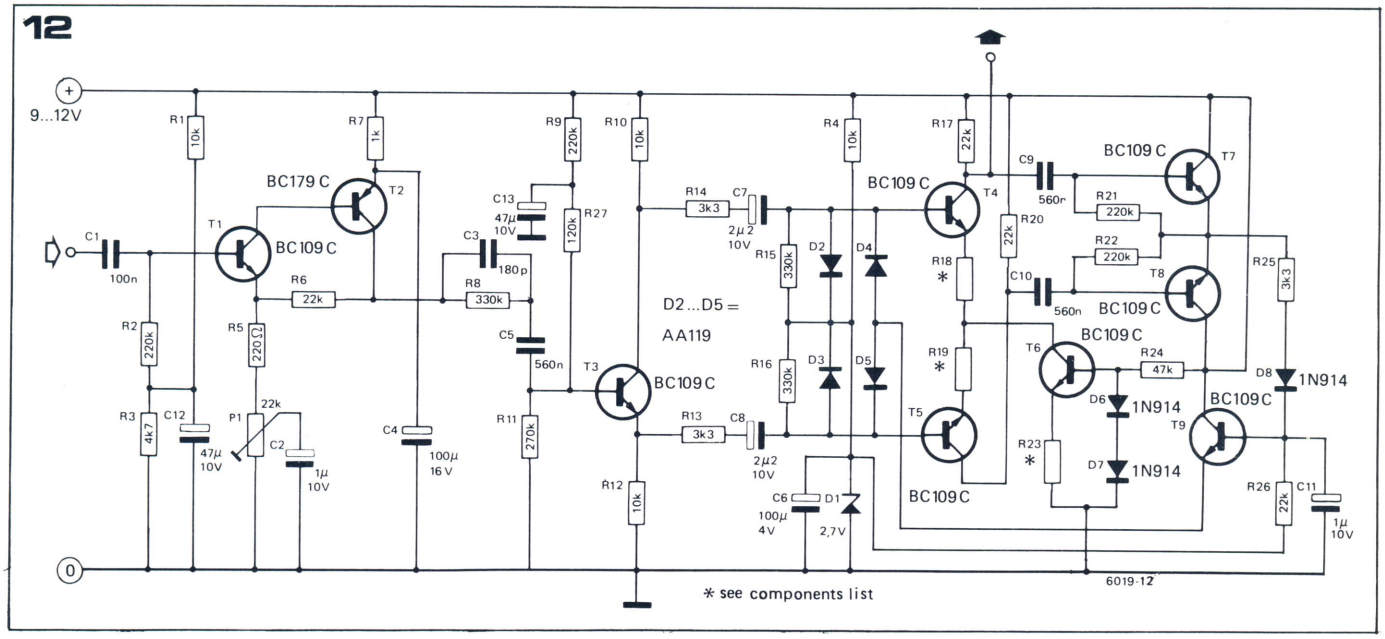

from the output of the attenuator and is also fed to a peak detector which rectifies the signal. The rectified voltage charges up the capacitor C via the potential divider consisting of R_1 and R_2. The time constant is $\frac{(R_1 + R_2)}{R_1.R_2}C$.

The voltage on C increases the attenuation of the voltage-controlled attenuator as the signal increases. If R_1 is small C charges up quickly but since the discharge path for C is via R_2 only, the decay time constant can be made as large as desired so that the voltage on C will not follow the signal waveform.

The voltage-controlled attenuator

Whilst the derivation of a control voltage from the signal is a relatively simple matter the design of a suitable voltage-controlled attenuator is another matter. Ideally the attenuator should be electrically isolated from the control voltage as otherwise the variations in control voltage with varying signal levels will appear as spurious noise at the output. One way of achieving this would be by using a light-dependent resistor (LDR) as the lower limb of the attenuator, as in figure 8. This would be controlled by a lamp driven from the control voltage.

Unfortunately problems arise due to the slow response of both the lamp and the LDR. Another rather elegant solution is to amplitude-modulate the signal onto a carrier and to vary the modulation depth by a voltage-controlled amplifier stage (figure 9). The compressed modulated signal is then filtered to remove control voltage noise and distortion (mainly second harmonic) and is then demodulated, resulting in a 'clean' compressed signal. Intermodulation distortion can still occur, but this can be minimised by proper circuit design.

The design chosen for the final circuit to be described was a diode attenuator. In its simplest form (figure 10) it suffers from two disadvantages.

1. The signal voltage will itself vary the attenuation as with a VDR thus causing distortion.
2. The control voltage will appear at the output superimposed on the signal thus producing spurious noise.

The first problem may be overcome by making the signal small compared with the control voltage so that it has little effect. The second may be prevented by using a balanced attenuator of four diodes as in figure 11. The signal appears differentially at the input of the differential amplifier and is therefore amplified. The control voltage, however, appears in common mode and is therefore rejected.

The Final Circuit

Figure 12 shows the circuit of a simple

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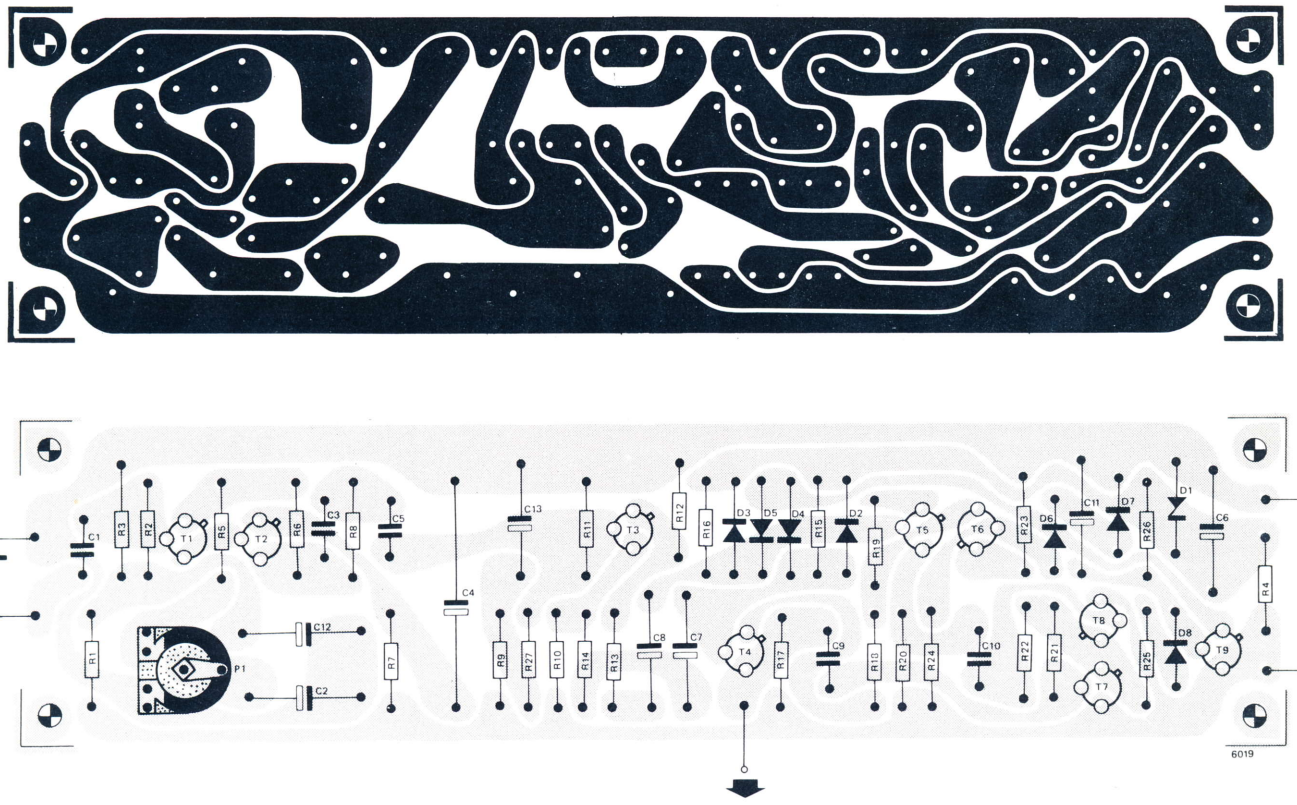

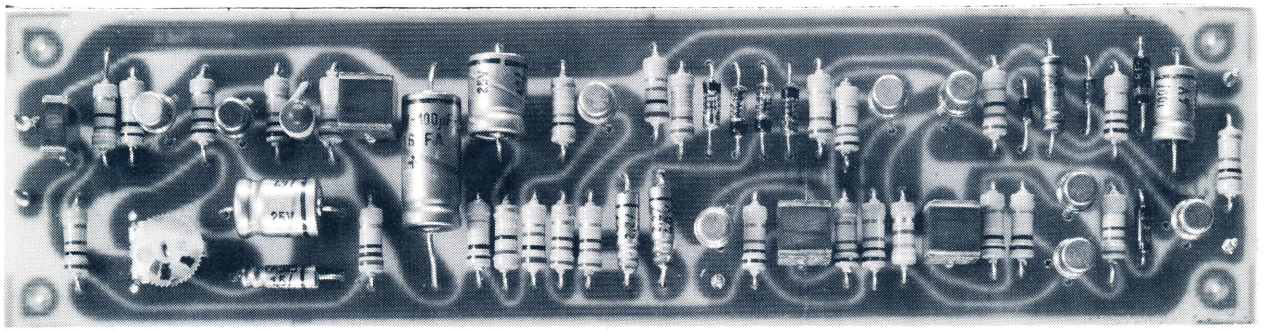

Compressor Specification

Input impedance	: 180 k
Output impedance	: 25 k (do not load with less than 100 k)
Gain with P_1 at minimum	: 60 (max. input voltage = 1 V)
Gain with P_1 at maximum	: 150 (max. input voltage = 30 mV)
Maximum (compressed) output voltage	: 500 mV
Maximum distortion (gain = 60)	
a. below compression threshold	: 0,4%
b. at maximum (1 V) input	: 5%
Maximum control current through diode bridge	: 350 μA
Power consumption	: 10 mA at 9 V

compressor intended principally for speech applications. The circuit has an input stage with adjustable gain which is sensitive enough to be driven by a magnetic microphone. This is followed by a phase splitter which produces two antiphase signals to feed into the differential stage T_4, T_5. The compressed output is taken from the collector of T_4 which should not be loaded with anything less than 100 k as this would upset the circuit operation. A class B-type stage T_7, T_8 drives the peak detector D_8, C_{11}. The control voltage appearing on C_{11} is buffered by the emitter follower T_9 and is fed to the diode bridge D_2 ... D_5. D_1 is a threshold control which determines the point at which compression starts. T_6 is simply a constant current source for the differential pair.

The board and component layout for the compressor are given in figure 13 and the performance figures in the table. At first sight it may seem that the distortion with the compressor operating is rather high but compared with the distortion when an amplifier is overloaded it is minimal.

Applications of the compressor

This compressor is sure to find a whole host of applications. It can be used to control the recording level in a tape recorder to prevent overloading of the tape. It can be used in amateur radio installations to achieve the largest possible modulation without overmodulating so that maximum range can be achieved. It can be used in a car radio so that quiet passages may be heard above the engine noise without loud passages being unbearable. The range of applications is limited only by the ingenuity of the constructor - remember, a compressor rules the waves (somewhat straighter than they were originally!).

Bibliography:

Electronic Engineering, January 1973.

Radio Elektronika, January 1959.

thief suppression in cars

Thefts of cars, or accessories and/or other articles in them, are becoming more and more common. By the same token, anti-theft alarms for cars are becoming more and more of a necessity . . . .

Each year an increasing number of cars are stolen. The majority of them are quickly recovered, but at best they have been abandoned on running out of petrol, and often they are a total write-off, with everything of value removed. Thefts of articles from cars are still more common, especially now that expensive in-car entertainment systems are so popular. When compared with the possible loss of property and/or no-claims bonus, the cost of installing a burglar alarm is negligible, and two designs are presented here, which should cost about 10 p and £ 10 respectively. Even with an alarm installed, however, do not ignore the simple precautions advised by the police. Lock all valuables in the boot, and make sure that all doors and windows are securely fastened.

A very simple alarm.

The simplest of the burglar alarms can be constructed from components that most enthusiasts will have in their junk box. It makes use of the door courtesy light switches and the horn relay, and the only additional components required are three diodes and a hidden switch to activate and de-activate the alarm. However, one door of the car is left unprotected.

The circuit operates as follows:

S_1 and S_2 are the courtesy light switches. When the hidden switch S_3 is closed, opening the door protected by S_2 causes the horn relay to operate via S_3, D2 and S_2. When the horn relay contacts close the horn sounds and the cathode of D3 is grounded via the relay contacts. This latches the horn relay via S_3 and its own contacts. The horn will continue to sound even if the door is closed, unless S_3 is opened. The door containing S_1 is, of course, not protected, as when S_1 is closed D1 is reverse biased and only the interior light operates.

When the alarm is not armed (S_3 open), D2 prevents the interior light from lighting when the horn button is pressed and D3 prevents the horn from sounding when the interior light is switched on.

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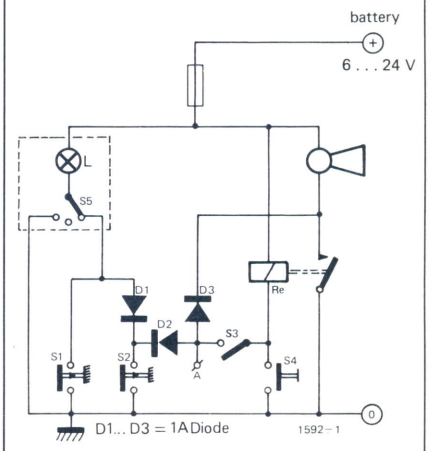

Figure 1. Circuit of the simplest burglar alarm consisting of three diodes and a switch. The door containing S_1 is not protected. Additional door switches should be wired in parallel with S_2, other switches such as boot and glove compartment between point A' and earth.

Figure 2. Block diagram of the sophisticated alarm.

Figure 3. Timing diagram of the alarm of figure 2.

Figure 4. Circuit of the sophisticated alarm, which uses COSMOS IC's.

Figure 4a. Alternative method of wiring the horn and horn relay, for cars with one side of the horn connected to chassis.

Additional courtesy light switches (in the case of a four-door car) may be connected in parallel with S_2, and switches to protect glove compartment and other ancillary equipment may be connected between point 'A' and ground.
This simple alarm will provide a fair degree of protection at little cost, but it should be noted that alarms which sound indefinitely after being triggered are illegal in some European countries.

A sophisticated alarm.

A block diagram of a more sophisticated burglar alarm system is given in figure 2. In many modern cars with a steering lock there is no need to have a concealed reset switch as a position is often available on the ignition switch that only opens when the switch is in the 'locked' position. It is thus possible, on entering the car, to de-activate the alarm by inserting the ignition key and turning it to the first position (without actually switching on the ignition). On cars without a steering lock, however, it will be necessary to use a separate concealed switch – or a separate lock-switch.

A timing diagram of the alarm is given in figure 3. On removing the ignition key from the lock the driver has about one-and-a-half minutes to leave the car and lock the doors. If a door is subsequently opened there is a delay (adjustable from 5 to 15 seconds) to allow the driver to reset the alarm with the ignition key. Failing this, the alarm operates and the horn will sound continuously for 30 seconds. After this there is ten seconds silence, then short three second blasts with ten seconds silence in between until the alarm is reset or the door is closed. The complete circuit of the alarm is given in figure 4.

When S_1 is opened C1 begins to discharge through R1 and R2. When the voltage on C1 falls below the threshold voltage of gate 2 then the flip-flop consisting of gates 1 and 2 is set.

This holds the input (pin 13) of gate 4a high, which means that when one of the door switches (represented by S_2) closes, the flip-flop consisting of gates 3a and 4a is set. The alarm is triggered, and even closing the door (opening S_2) will not reset the flip-flop. C2 and C3 were previously charged through R6 and D3 from the output of gate 1a. C2 and C3 now discharge through R5 into the output of gate 4a. C3 may be optionally switched in by S_3 to increase the delay before the alarm sounds. With S_3 closed the delay is about 15 seconds; with S_3 open the delay is only 5 seconds. If this facility is not required S_3 and C3 may be omitted and C2 replaced by a capacitor chosen to give the required delay.

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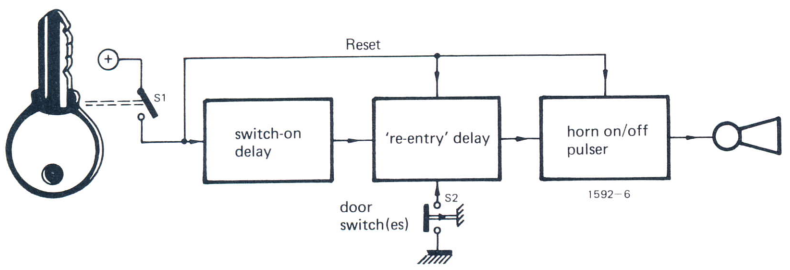

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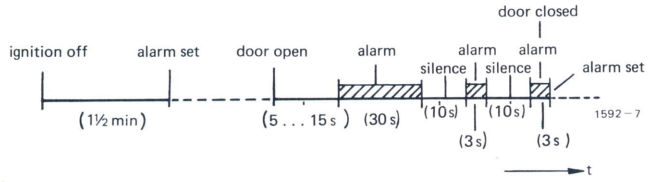
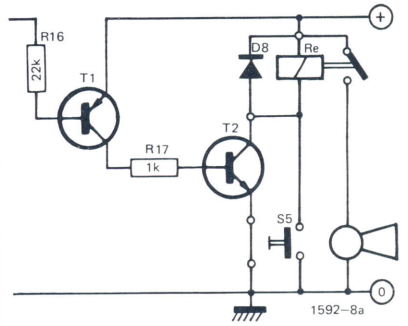


4a



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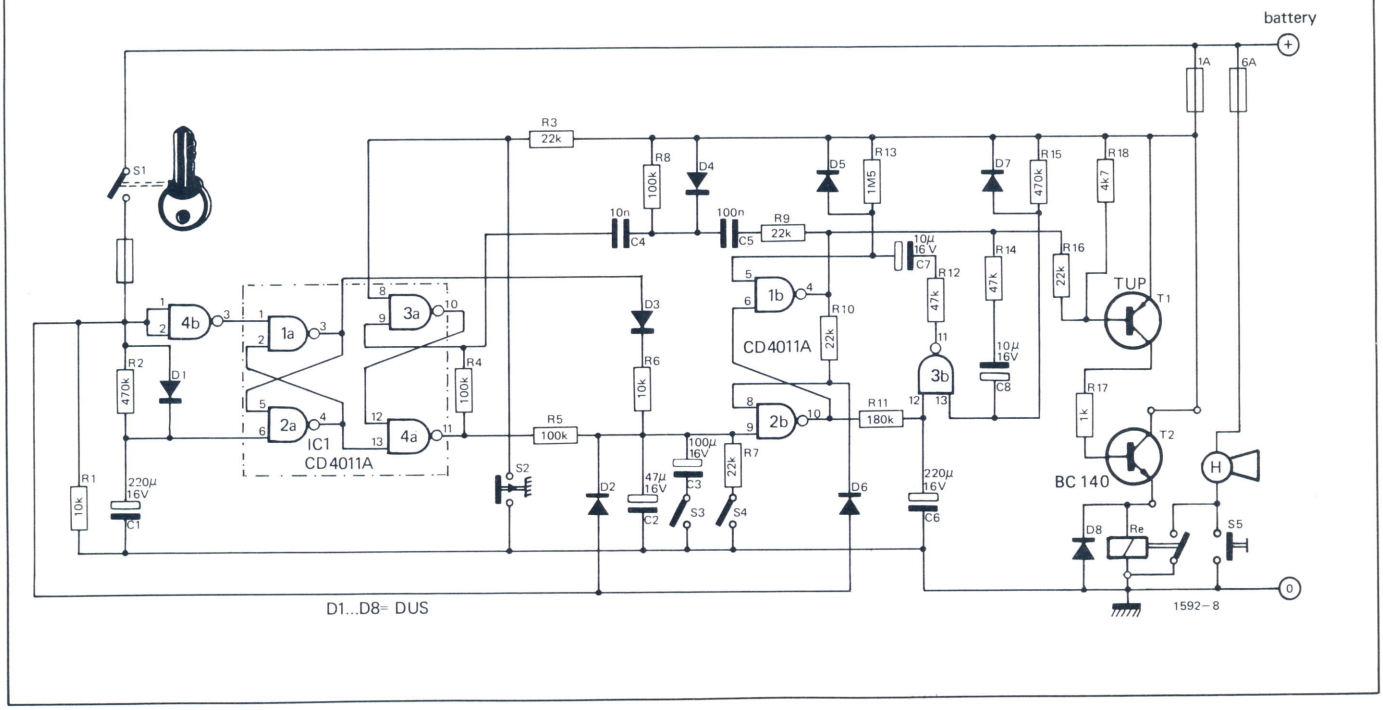


S_4 may be a trembler switch or switch(es) on glove compartment, boot etc., which will discharge C2 and C3 rapidly and trigger the alarm.

When C2 and C3 have discharged the output of gate 2b goes high. This takes pin 6 of gate 1b high. Since the other input is held high by R13 the output goes low, turning on T1 and T2 and sounding the horn. C8 charges through R14 and R15 in about 3 seconds, taking pin 13 of gate 3b high. Meanwhile C6 slowly charges through R11 and it is this time constant that determines the duration of the initial blast of the horn (about 30 seconds).

When the voltage on C6 exceeds the threshold voltage of gate 3b the output of this gate goes low, grounding pin 5 of gate 1b through C7 and R12. The output of 1b thus goes high and the horn switches off. C8 now discharges through D7, R14 and the output of gate 1b. C7 slowly charges through R13 and R12, and this time constant determines the 'off' period of the horn (about 10 seconds). When C7 has charged to the threshold voltage of gate 1b the output goes low and the horn again sounds. C8 charges through R14 and R15, and this time constant determines the subsequent 'on' periods of the horn (about 3 seconds).

After this period the output of 3b goes low, grounding pin 5 of gate 1b through R12 and C7, and the whole cycle repeats.

Gates 1b and 3b thus form an asymmetric multivibrator which causes the horn to produce short blasts at 10 second intervals. In addition, each time the horn is switched off a differentiating network consisting of R8, R9, C4 and C5 feeds a reset pulse to pin 9 of gate 3a, so that if the doors are closed during the horn 'off' period, the horn will not sound again and the alarm will be re-set.

The only disadvantage of this alarm circuit is that it cannot easily be adapted for positive earth cars. On the other hand, it has the advantage that it is insensitive to spurious pulses due to the high noise immunity of COSMOS. The circuit will operate over a wide range of supply voltages without modification (4 to 14 volts), with almost the same delays.

Installation of the alarm

To ensure reliable operation the alarm should be mounted where it cannot be disabled by a thief, but not inside the engine compartment, which gets rather hot for COSMOS. Wiring should be concealed or made as inconspicuous as possible, especially wiring into the engine compartment if the car does not have a bonnet lock. In this case it is also wise to install an alarm switch in the bonnet lid, as otherwise the alarm could be disabled simply by disconnecting the battery. Another (somewhat expensive) possibility would be to power the alarm from a separate battery locked in the boot. Wiring from the battery to the alarm should, of course, be direct, not via the ignition switch, and the simplest way is to run cables from the battery side of the fuse box with in-line fuse holders in them.

When constructing either of these alarms it should be borne in mind that they may need to be adapted to suit particular types of car. For instance, some horn relays have one end of the coil and the contact commoned, so they would not work in the circuit of figure 1. A separate heavy-duty relay (6A contacts) would have to be used. This problem does not arise with the more sophisticated design, and a normal horn relay may be used. A printed circuit board layout is given in figure 5 for the alarm circuit of figure 4 and this has alternative sets of connections for the relay, as shown in figure 4a, to suit different car wiring. S_5 in both circuits is the original pushbutton for the horn.

Final Remarks

The designs discussed in this article give varying degrees of protection at varying cost. It should be remembered that any protection is better than none – the majority of thieves are amateurs and will be deterred by even the simpler circuit described.

5

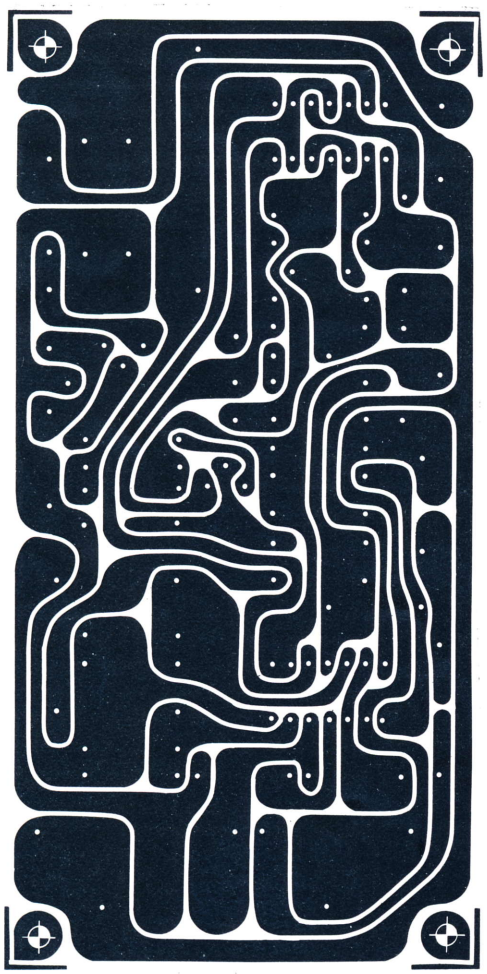
Components list for figures 4 and 5.

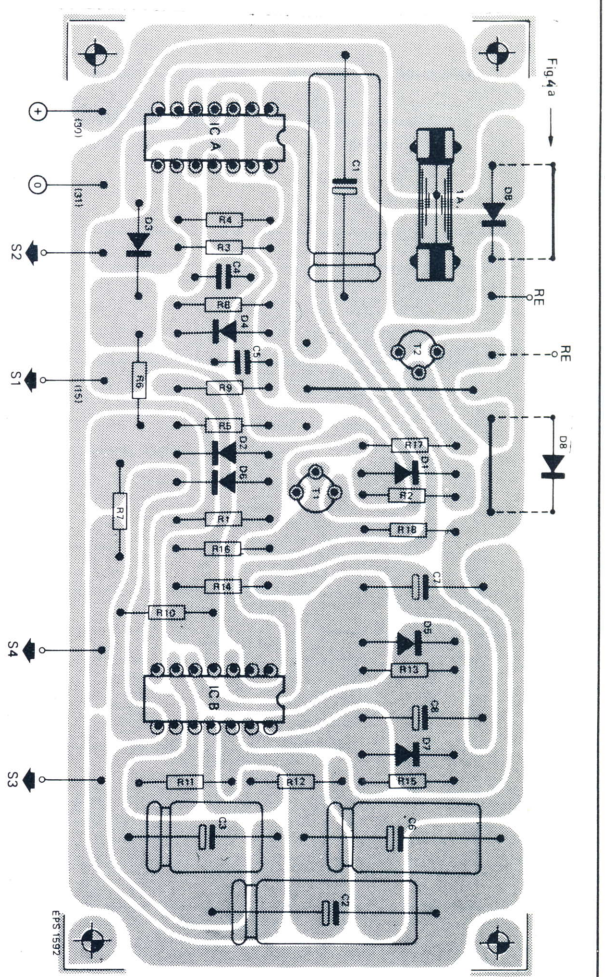
Resistors:
R1,R6 = 10 k
R2,R15 = 470 k
R3,R7,R9,R10,R16 = 22 k
R4,R5,R8 = 100 k
R11 = 180 k
R12,R14 = 47 k
R13 = 1M5
R17 = 1 k
R18 = 4k7

Capacitors:
C1,C6 = 220 µ/16 V
C2 = 47 µ/16 V
C3 = 100 µ/16 V
C4 = 10 n
C5 = 100 n
C7,C8 = 10 µ/16 V

Semiconductors:
ICa,ICb = CD4011A
T1 = TUP
T2 = BC140 or equ.
D1 . . . D8 = DUS

Figure 5. Board and component layout for figure 4.





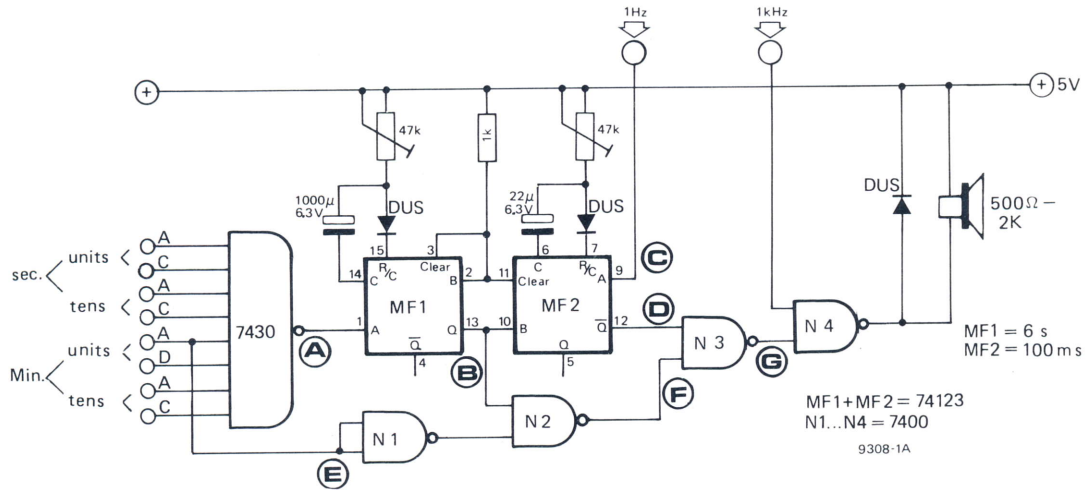
time signal simulator

the logic '1' level only being used for decoding. The code shown in the diagram corresponds to the moment 59'55''. The period of MF1 monostable is about 6 seconds. During this period monostable MF2 is triggered by a 1 Hz signal at (C), as shown in the pulse diagram, its B input being logic '1' (B). The MF2 monostable period has been set to about 100 millisec, which permits MF2 to be triggered every second. The result is a signal at (D).

Until the turn of the hour, the minute-unit mark remains logic '1' (E). N1 marked by a 'pip' of a length of about 1 second.

The tone itself appears at the input of N4. If the clock is crystal controlled it may be possible to derive a frequency of around 1 kHz from the divider circuitry in the clock. Otherwise a simple 1 kHz multivibrator may be used.

1a

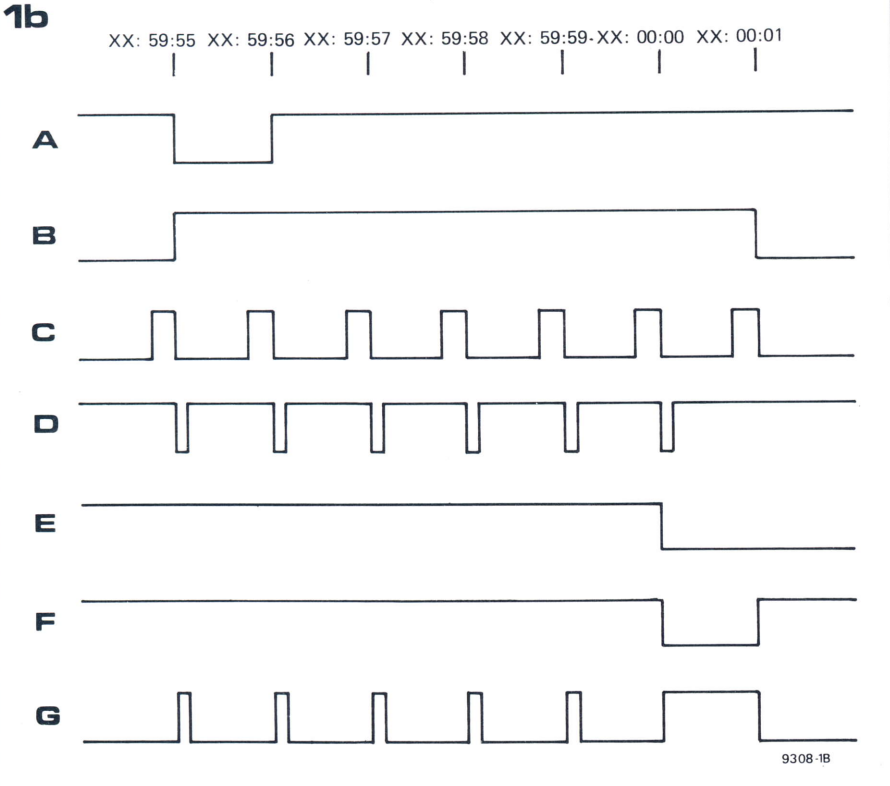


This circuit generates a 'six pips' signal indicating the exact hour.

At the instant the first 'pip' is to start, an eight-input NAND gate, which receives BCD-coded minute and second marks from a TTL clock, transmits a negative-going edge to MF1 (at A). Each digit requires not more than two inputs, inverts this level, causing the signal at (F) also to be '1'.

At the instant 00'00'', N2 by-passes MF2. This means that MF2 only determines the length of the first five 'pips'. The length of the sixth 'pip' is determined by the remainder of the MF1 period (G). The new hour is, thus,

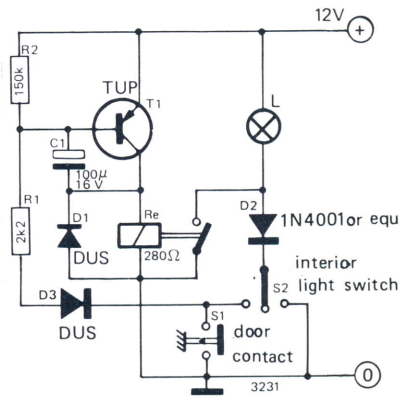
1b



afterburner

W. Ferdinand

When starting a car journey after dark it is useful to have a device which will keep the interior lighting on for a while after the doors have been closed, and so make it easier for the occupants to fasten safety belts and insert the ignition key. This can be done with the simple time-switch circuit shown.



A. Seitz

fido

Fido is a new electronic game in which an unfortunate dog is called by four masters at the same time. The command "Fido come" is given by means of a pushbutton. At each push on one of the four buttons controlled by each player Fido jumps in the required direction. However, the four masters and/or mistresses have one handicap: After one successful command to Fido, the would-be Fido owner who has given the order has nothing more to say for a certain time. Then the other players can go on with Fido. If one of the players succeeds in getting Fido into his kennel, the game is decided: Fido stays where he is.

Construction and operation

Since Fido is clever enough to let himself be represented by a small incandescent lamp, he is not going to suffer from an otherwise unavoidable nervous breakdown. The worst that can happen is that after a prolonged fight for mastery over Fido our doggy will suffer from a flat battery.

On the playing board nine lamps are arranged in a square (figure 1). On the extension of each side there is a lamp representing a kennel (so in total four). Furthermore, at each of the corners there are four push buttons with a pilot lamp to indicate when a player can join the game. The buttons make Fido jump in four directions (away, towards, left or right with respect to the particular player). The photograph also shows that the "gaming table" is provided with an on/off switch, an interval switch (coarse) and an interval control (fine) for setting the obligatory rest period for the players. These switches can be calibrated "bloodhound/whippet" and "dog-tired ... alert" respectively.

Furthermore there is a switch to disable the "rest" lamps and there is also a starting switch By pushing this button, Fido takes up his position in the centre of the field; i.e. the middle lamp is alight. By pushing one of his buttons, each player can now try to direct Fido into his kennel. Once a player has pushed a button, he is obliged to take a breather before he can push a button again. The lamps fitted near the buttons indicate when the next command can be given. Each player can give only one command at a time. If an impatient player pushes his button too soon, the penalty is a new start of the waiting period. So Fido will not respond to a command that comes too early.

To make the game a bit more exciting, the pilot lamps can be switched off, so that each player must just guess when he may next give a command.

The block diagram

Fido's position in the field is indicated by nine lamps arranged in a square. These lamps are located at the intersections of 3 X 3 matrix rails. The signals for these rails are driven by two left/right shift registers. The clock pulses to the registers are produced by the players pushing one of the buttons. Since each player has four buttons at his disposal, Fido can be sent in all directions including the kennel of another player.

The directing signals for left, right, up and down are coupled into the registers via the multiplexer. Once in a corner, the dog can be made to jump into the kennel situated below the corners as seen from the player's position. The register input driving the "kennel" flipflop is so connected that the command for jumping is only followed if the other register, too, is in the proper position. The lamp field is blocked to prevent lamps from lighting up after a jump into the kennel. At the same time all register outputs are blocked so that no more "kennel" flipflops can be driven.

The game is started by pushing the starting button; then all the "kennel" flipflops are reset and the two shift registers take up a central position. In that case the middle lamp is alight.

The left/right shift register

Figure 3 shows how a flipflop can be turned into a "flipflopflap". The inputs of each nand are connected to the outputs of the other nands. Consequently, only one output at a time can be low ("0"). This "0"-signal produces a high output level ("1") at all the other nands; these high levels in turn cause the low output level on the first nand. A negative-going pulse on one of the coupling rails causes all nands connected to this rail to change to "1", whereas the nand whose output is connected to this rail ensures that this rail remains "0".

If gates with a so-called totem-pole output are used (7400, 7420 and 7430) the outputs must be separated by means of a diode as otherwise none of the

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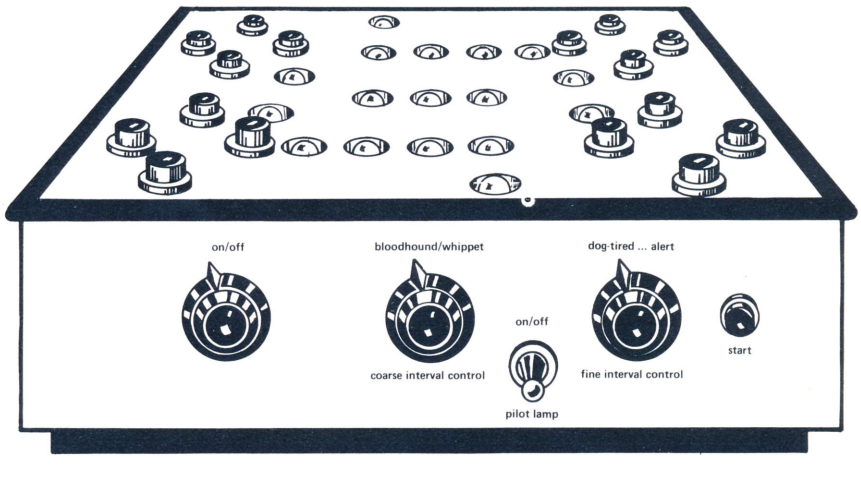
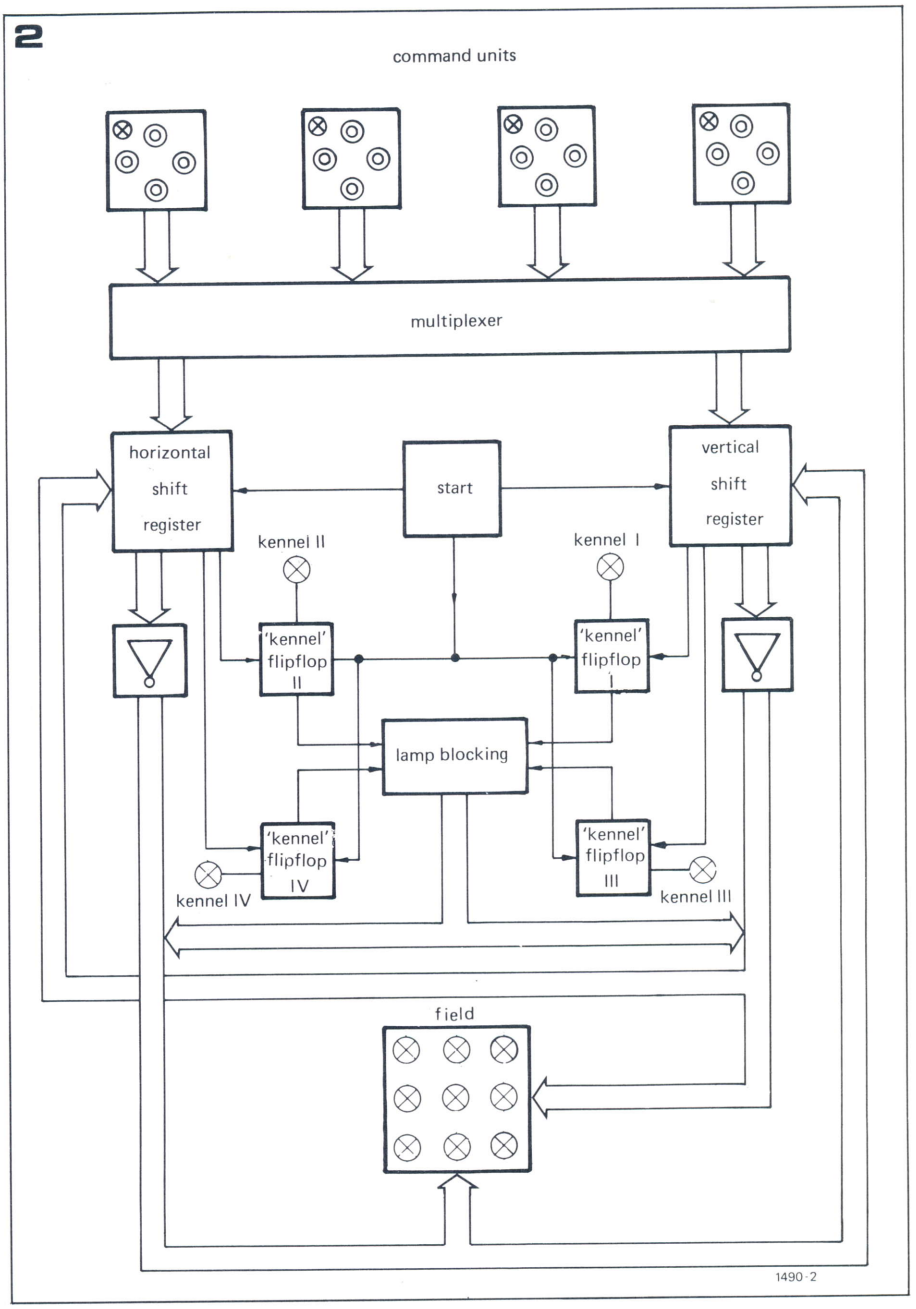


Figure 1. Artist's impression of Fido.

Figure 2. The block diagram. The command-units also comprise the waiting time indication. The push button "start" resets all "kennel" flipflops and sets the registers at the central positions, so that the lamp in the center of the field lights up. Multiple connections between the circuits are indicated by means of broad arrows.

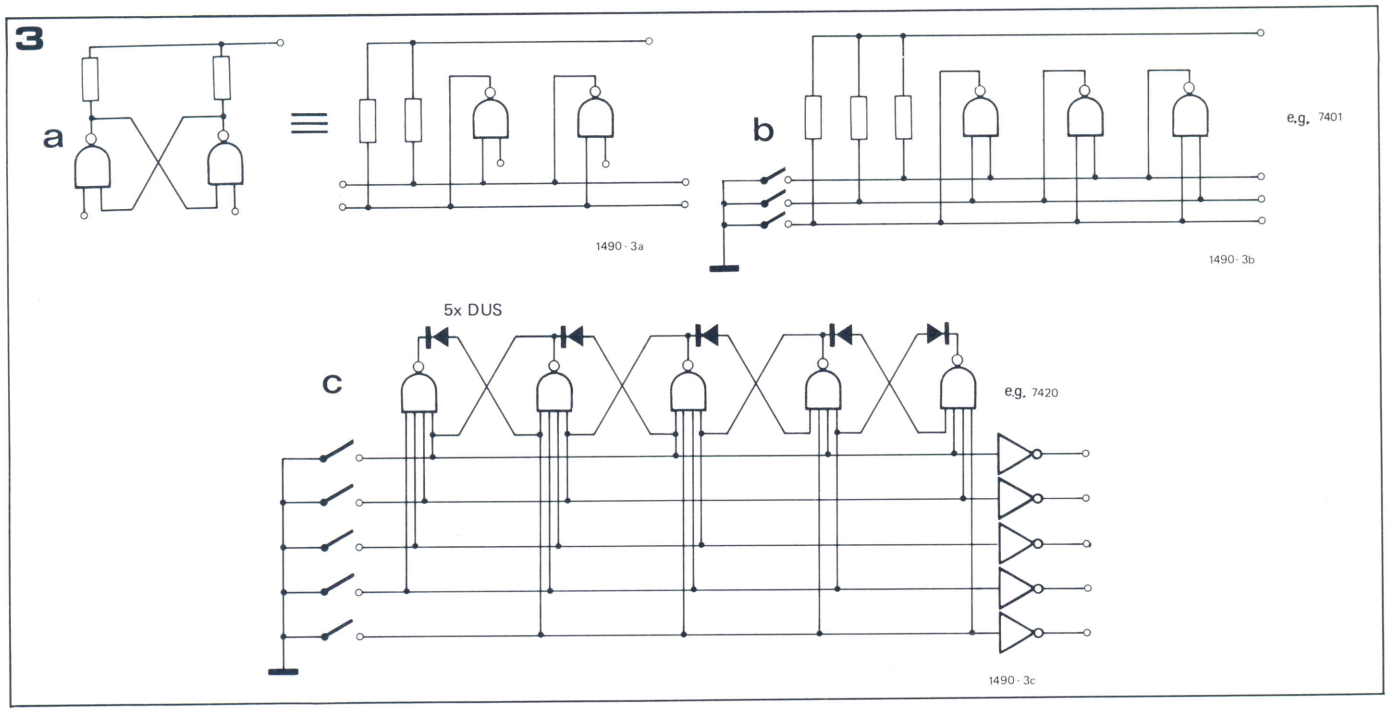
Figure 3. The development of a multiple flipflop starting from the fundamental principle.
a. Two methods of drawing a simple flipflop
b. A 3-fold flipflop
c. A 5-fold flipflop.

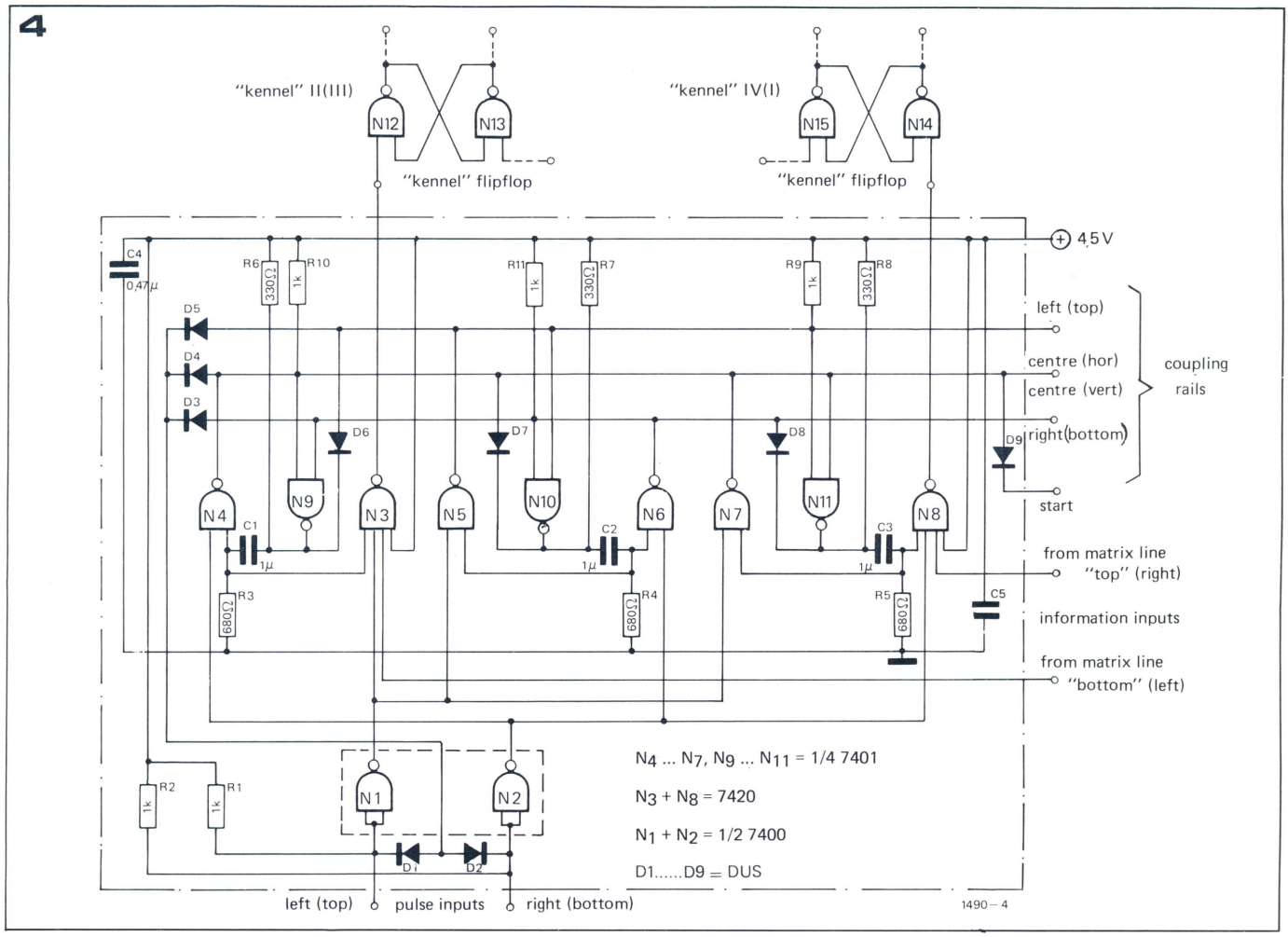


outputs would change to low (figure 3c). With types with an open collector output this is not strictly necessary, although it is recommended to keep the input load of the pulse low.

In that case the "0" must, after each pulse, shift one position to the right, left, top or bottom. So we need a memory which remembers what coupling rail is carrying a "0" signal before the pulse, and a circuit that determines in what direction the shift should take place.

The memory is formed by C_1, (C_2, C_3, figure 4); the direction of shift is determined by two nands (N_3 and N_4, N_5 and N_6, N_7 and N_8) which receive their signals via N_1 and N_2. When the button is pushed, say left, this is what happens: Via N_1, connected as an inverter, the "1" signal is fed to the nands N_3, N_5 and N_7 via the "left" conductor. At the same time all the connecting rails are brought to the "0" level via the diodes D_1, D_3, D_4 and D_5. As a result, the nand N_9,





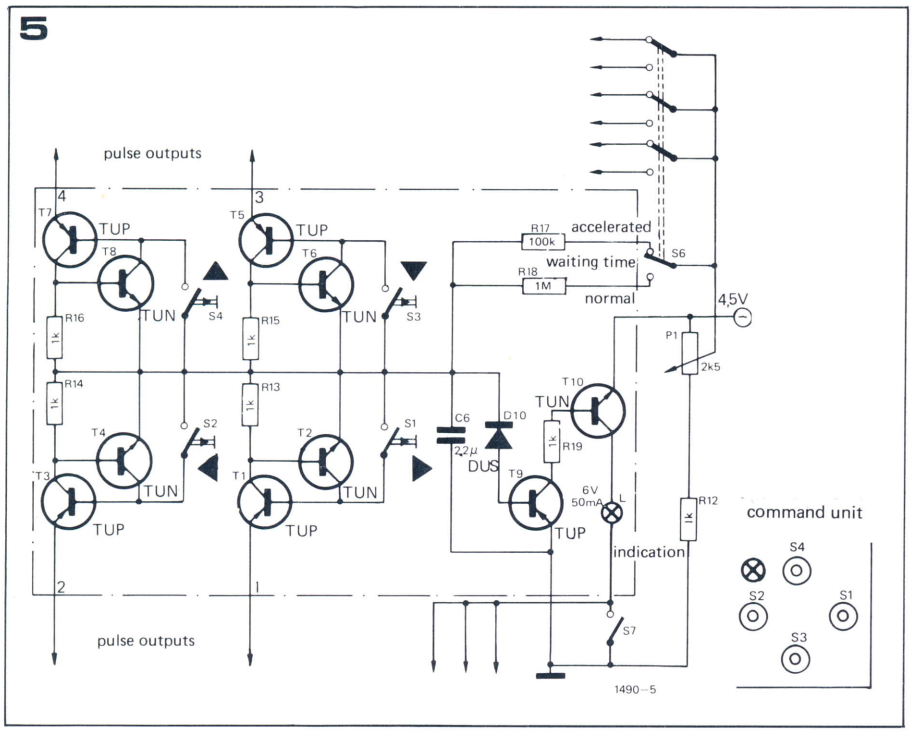


Figure 4. Complete "shift register for a zero", 3-fold, for the matrix line of the horizontal shift register. The vertical register is of the same construction (description between brackets).

Figure 5. Field with waiting time indication. Depending on the type of field used, the trigger unit is required several times. It serves to suppress contact bounce.

Figure 6. Diagram for Fido with nine lamps. If the whole is fed from batteries, it is advisable to supply the lamps from a separate battery because pulses caused by switching (low filament resistance of an extinguished lamp) might interfere with the circuit. The bias of C_6 (figure 5) must also be obtained from a separate battery because a maximum current of about 200 mA can occur.

N_{10} or N_{11}, which has been at "0" level so far, changes to "1". Simultaneously, a positive pulse is fed to the two adjacent nands via the capacitor connected to this output. The gate thus prepared by the "1" signal via the conductor "left" maintains the collecting line of its neighbour at "0" until again via diode D_1 the "0" signal disappears and the remaining conductors become logically "1".

The contact potentials of the diodes D_1 and D_3 up to and including D_5 ensure that the coupling rails reach the "1" potential before the inputs of the gates 1 or 2. This is necessary to ensure that the new main nand takes over the "0" signal before the direction determining gate changes back to "1".

In the extreme positions for the "shift register for a zero", the "kennel"-flipflops N_{12}-N_{13} and N_{14}-N_{15} are driven. These may be driven only when the second register reports the correct position. The outer direction determining gates N_3 and N_8, which drive the "kennel" flipflops require three inputs for that purpose; one being coupled to the corre-

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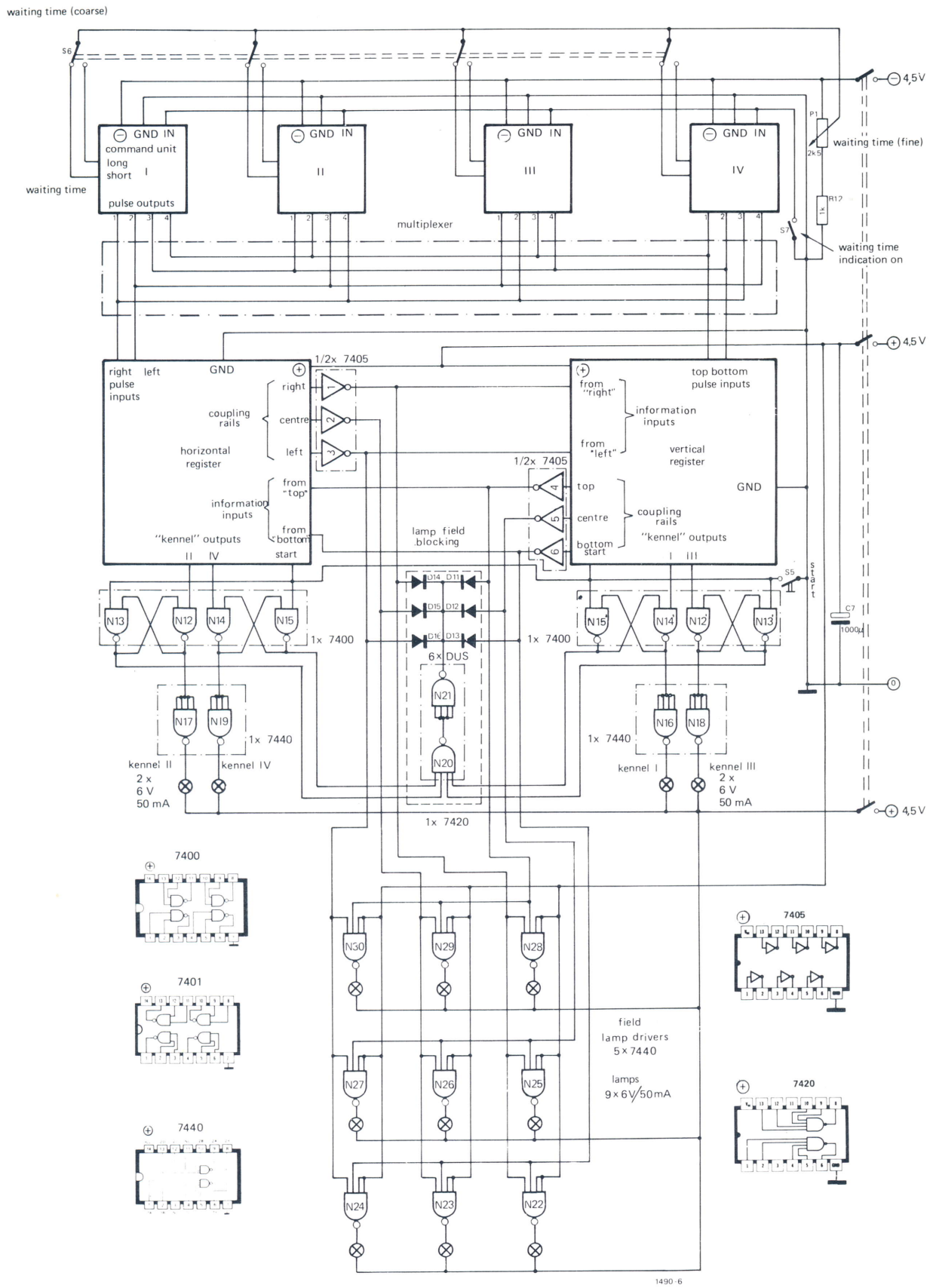

sponding matrix line of the other register.

Command-unit with indication

Figure 5 shows a command-unit with four push buttons. The other units are similar.

Via P_1 and R_{17} or R_{18}, respectively, capacitor C_6 is negatively charged until the voltage across C_6 equals the sum of the contact potentials of diode D_{10} and the base-emitter junction of T_9. The latter is then conductive, so that T_{10} causes the lamp to light up. The pilot lamp indicates when a command can be given. The waiting time can be adjusted with P_1.

When pushing a button, say S_1, T_1 is turned on by the negatively charged capacitor C_6, so that the emitter of T_1 drops from +4,5 V to +0,7 V. This pulse serves to drive the shift register.

Due to contact bounce, Fido is likely to make wild and unpredictable jumps, or just stays where he is. To avoid such "disobedience", each push button must be connected to a trigger. Even the shortest pulse at the base of T_1 is suffi-

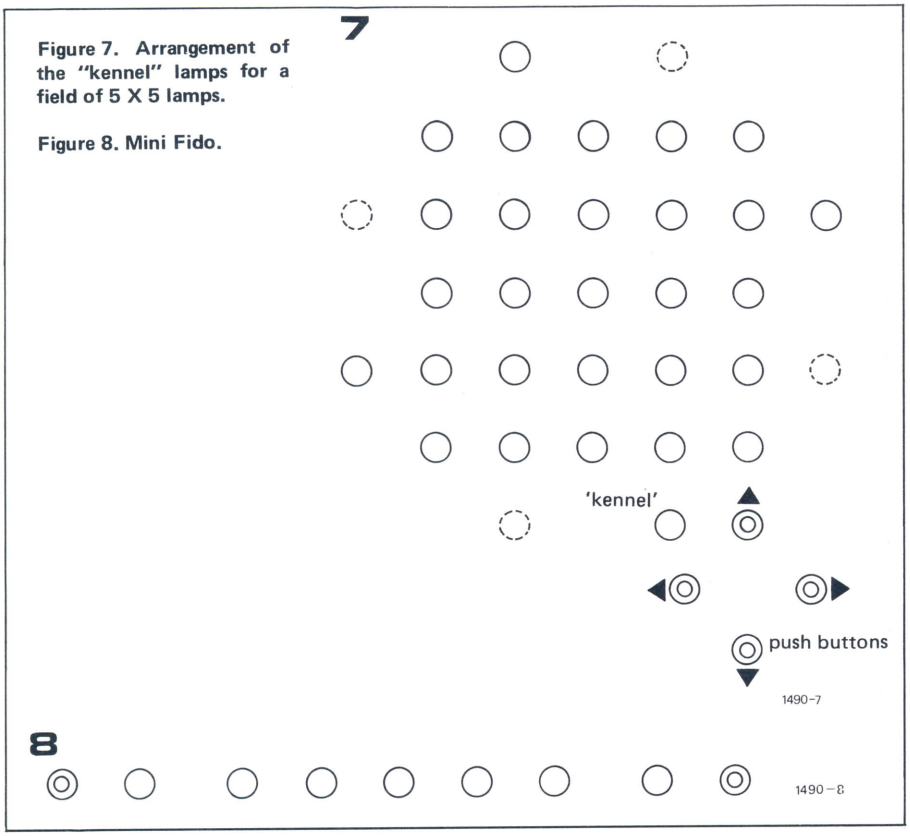

Figure 7. Arrangement of the "kennel" lamps for a field of 5 X 5 lamps.

Figure 8. Mini Fido.

cient to cause the two transistors (T_1 and T_2) to switch. As a result capacitor C_6 is connected to the control line until the voltage drop across R_{13} caused by the charge current is no longer high enough, and the trigger returns to its initial position. Then capacitor C_6 discharges across R_{17} (R_{18}) and P_1.

The complete diagram

Owing to the large extent of the circuit, some of the sections are represented as blocks in figure 6. The positions indicated by the coupling rails are represented by "0"-signals. For the remainder, only "1"-signals are used; hence the inverters 7405 for inverting the signals. These signals are fed to the lamp drivers 7440 which cause the lamps to light up when all inputs are "1".

Since only two of the four inputs of the lamp drivers are used, all the others can be connected to the positive of the supply, which, however, is not necessary.

Once Fido has disappeared into a kennel, that is to say: when a "0" signal has reached the input of a goal flipflop, a "1" is produced at the driver of the goal lamp, and a "0" at the gate N_{20}, which via the inverter N_{21} and six diodes D_{11} up to and including D_{16} transfers this signal to the outputs of the inverters I_1 up to and including I_6. As a result all the lamps in the field are extinguished. Furthermore, all the outer direction-determining gates (figure 4) are blocked ("0"-signal at the inputs that are connected with the inverter outputs), so that no further goal can be scored by the now invisible Fido, if more buttons were pushed.

The start- or reset button returns the goal flipflops and the registers to their initial positions again. The middle coupling rails must be connected to the reset conductor via the diodes (D_9 in figure 4). The words "left", "right", "top", "bottom", "vertical" and "horizontal" are related to a group of push buttons which is fixed by an arbitrary position of a player and is called command-unit 1. The other command-units are numbered clock-wise. The arrows in figure 5 are related to the way in which Fido moves as regards the player concerned.

Variations

The game can easily be changed. A first possibility is to expand the field so that the game will last longer (figure 7, according to the principle in figure 3c). This will, of course, increase the cost of the unit by a considerable amount, especially if the 25 lamp version of figure 7 is used. Furthermore, it should be noted that the field is in fact only suitable for four or eight players, whereas the smaller field can also be used by two without Fido endlessly running up and down.

On the other hand, the field with 25 lamps can easily be connected to eight command-units, so that eight "dog lovers" can join the game.

A "mini Fido" is also a possibility if we restrict ourselves to one register (see figure 3c), and if the "kennels" are placed at the two ends of the row of lamps (figure 8). In spite of the simple set-up the game can still be fun; playing with the push buttons alone is most amusing. In addition this version offers the possibility of studying the register.

Of course, other possibilities can be worked out, but then again it is up to the reader to find an arrangement in accordance with his taste and, lets face it, budget.

elektor services to readers

EPS print service

Many elektor circuits are accompanied by printed circuit designs. Some of these designs – but not all! – are also available as ready-etched and predrilled boards, which can be ordered from our Canterbury office. A complete list of the available boards is published under the heading 'EPS print service' in every issue. Delivery time is approximately three weeks.

As a further service, boards which are taken off the regular service list at some future date will continue to be available in spite of this; delivery time will then be approximately six weeks. It should be noted, however, that only boards which have at some time been published in the EPS list are available; the fact that a design for a board is published in a particular article does not necessarily imply that it can be supplied by elektor.

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Members of the technical staff will be available to answer technical queries (relating to articles published in elektor) by telephone on Mondays from 14.00 to 16.30. Queries will not normally be answered at other times.

Letters should be addressed to the department concerned: TQ = Technical Queries. Although we feel that this is an essential service to readers, we regret that certain restrictions are necessary:

1. Questions that are not related to articles published in elektor cannot be answered.
2. Questions concerning the connection of elektor designs to other units (e.g. existing equipment) cannot normally be answered, owing to a lack of practical experience with those other units. An answer can only be based on a comparison of our design specifications with those of the other equipment.
3. Hieroglyphs or illegible handwriting cannot be decoded; provided the sender's address is legible, the letter is returned unanswered.
4. Questions about suppliers for components are usually answered on the basis of advertisements, and readers can usually check these themselves.
5. As far as possible, answers will be on standard reply forms.

We trust that our readers will understand the reasons for these restrictions. On the one hand we feel that all technical queries should be answered as quickly and completely as possible; on the other hand this must not lead to overloading of our technical staff as this could lead to blown fuses and reduced quality in future issues ...

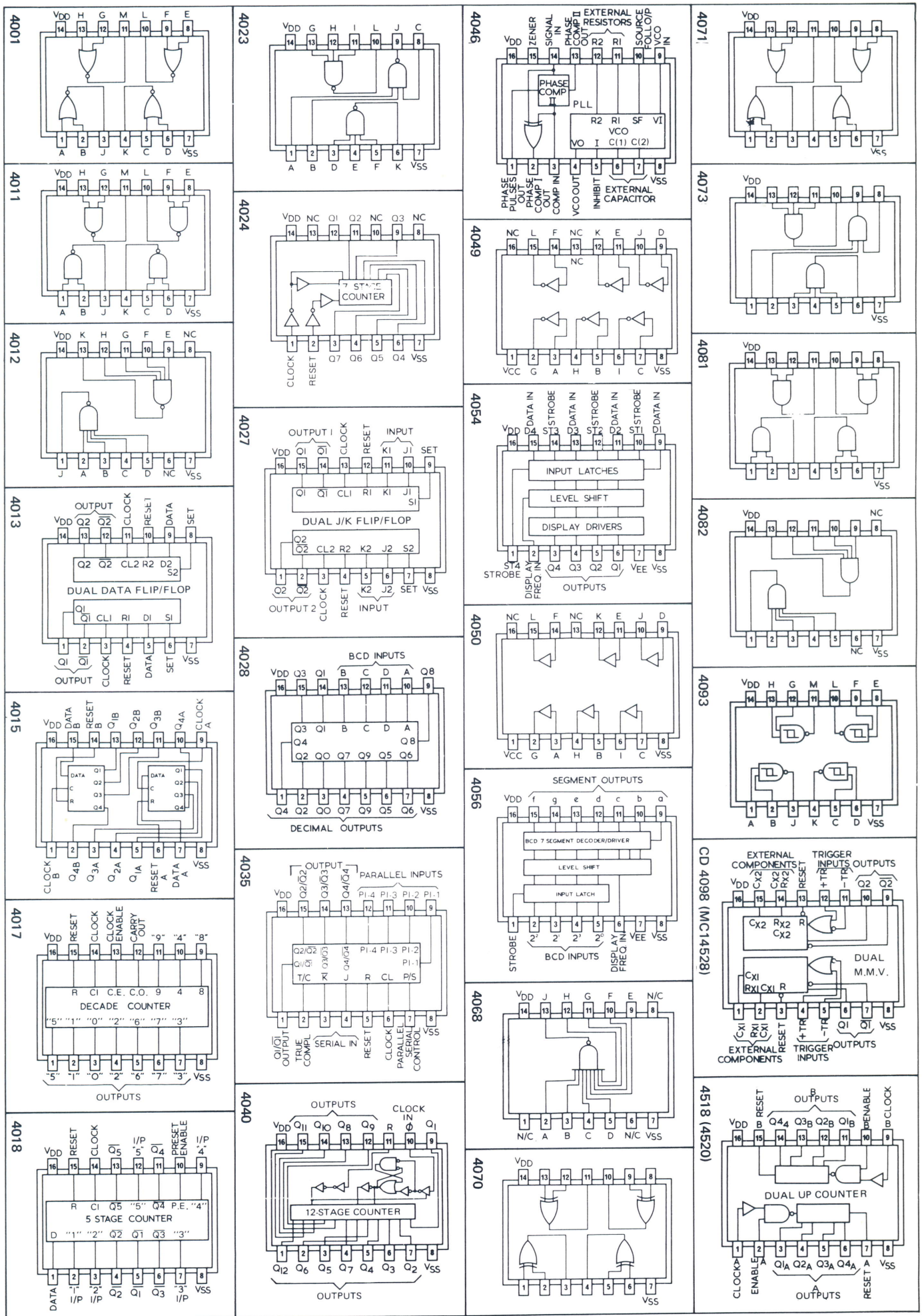
Manufacturer	Type number	Colour	Pin Function														Performance Data					Maximum Ratings				Dimensions			h
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	λ_p	I_v	V_{fs}	V_{fd}	@I_f	V_{rs}	V_{rd}	I_{av}	P_{tot}	W	H	D	
Boss	BIM-72R	Red	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	697	0.25	1.9	1 9	10	5	5	25	400	10	19	4.6	7.7
Boss	BIM-52G	Green	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	560	0.25	1.9	1.9	10	5	5	25	400	10	19	4.6	7.7
Boss	BIM-82Y	Yellow	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	580	0.25	1.9	1.9	10	5	5	25	400	10	19	4.6	7.7
Dialco	745-0006	Red	a	f	A	np	np	L	e	d	A	c	g	np	b	A	650	——	3.2	1.6	20	6	3	30	380	10	19	3.0	6.9
EEP	EP1	Red	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	690	1.0	2.1	2.1	15	5.5	5.5	40	750	10	19	3.2	8.5
EEP	EP21	Red	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	697	0.25	1.9	1.9	10	5	5	25	400	10	19	4.6	7.7
EEP	EP21G	Green	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	560	0.25	1.9	1.9	10	5	5	25	400	10	19	4.6	7.7
EEP	EP21Y	Yellow	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	580	0.25	1.9	1.9	10	5	5	25	400	10	19	4.6	7.7
EEP	EP27	Red	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	690	0.30	2.2	2.2	20	3	3	40	750	10	19	3.2	8.5
EEP	EP28	Red	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	690	0.60	2.2	2.2	20	3	3	40	750	10	19	3.2	8.5
Hewlett-Packard	5082-7730	Red	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	655	0.25	1.6	1.6	20	6	6	25	400	10	19	4.6	7.6
Hewlett-Packard	5082-7731	Red	a	f	A	np	np	nc	e	d	R	c	g	np	b	A	655	0.25	1.6	1.6	20	6	6	25	400	10	19	4.6	7.6
Hewlett-Packard	5082-7750	Red	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	655	0.25	1.6	1.6	20	6	6	25	400	13	19	6.4	11.0
Hewlett-Packard	5082-7751	Red	a	f	A	np	np	nc	e	d	R	c	g	np	b	A	655	0.25	1.6	1.6	20	6	6	25	400	13	19	6.4	11.0
Litronix	DL1A	Red	a	f	A	nc	nc	L	e	d	A	c	g	nc	b	A	630	——	3.4	1.6	20	6	3	30	750	10	19	3.0	6.9
Litronix	DL10	Red	a	f	A	nc	nc	L	e	d	A	c	g	nc	b	A	630	——	3.4	1.6	20	6	3	30	750	10	19	3.0	6.9
Litronix	DL10A	Red	a	f	A	nc	nc	L	e	d	A	c	g	nc	b	A	630	——	3.4	1.6	20	6	3	25	650	10	19	3.0	6.9
Litronix	DL707	Red	a	f	A	nc	nc	L	e	d	A	c	g	nc	b	A	630	1.4	1.7	1.7	20	3	3	30	500	11	20	7.4	7.6
Litronix	DL707R	Red	a	f	A	nc	nc	R	e	d	A	c	g	nc	b	A	630	1.4	1.7	1.7	20	3	3	30	500	11	20	7.4	7.6
Monsanto	MAN1	Red	a	f	A	nc	nc	L	e	d	A	c	g	nc	b	A	630	——	3.4	1.6	20	6	3	30	750	10	19	3.0	6.9
Monsanto	MAN1A	Red	a	f	A	nc	nc	L	e	d	A	c	g	nc	b	A	630	——	3.4	1.6	20	6	3	30	750	10	19	3.0	6.9
Monsanto	MAN5	Green	a	f	A	np	np	L	e	d	A	c	g	np	b	A	565	0.23	2.5	2.5	20	3	3	40	960	11	20	5.8	6.9
Monsanto	MAN7	Red	a	f	A	np	np	L	e	d	A	c	g	np	b	A	630	0.2	2.0	2.0	20	5	5	30	960	11	20	5.8	6.9
Monsanto	MAN8	Yellow	a	f	A	np	np	L	e	d	A	c	g	np	b	A	589	0.25	2.5	2.5	20	6	3	40	960	11	20	5.8	6.9
Monsanto	MAN51	Green	a	f	A	np	np	R	e	d	A	c	g	np	b	A	565	0.32	2.5	2.5	20	3	3	30	700	10	20	5.0	7.6
Monsanto	MAN52	Green	a	f	A	np	np	L	e	d	A	c	g	np	b	A	565	0.32	2.5	2.5	20	3	3	30	700	10	20	5.0	7.6
Monsanto	MAN71	Red	a	f	A	np	np	R	e	d	A	c	g	np	b	A	650	0.30	1.6	1.6	20	5	5	30	700	10	20	5.0	7.6
Monsanto	MAN72	Red	a	f	A	np	np	L	e	d	A	c	g	np	b	A	650	0.30	1.6	1.6	20	5	5	30	700	10	20	5.0	7.6
Monsanto	MAN81	Yellow	a	f	A	np	np	R	e	d	A	c	g	np	b	A	590	0.34	2.5	2.5	20	3	3	30	700	10	20	5.0	7.6
Monsanto	MAN82	Yellow	a	f	A	np	np	L	e	d	A	c	g	np	b	A	590	0.34	2.5	2.5	20	3	3	30	700	10	20	5.0	7.6
Monsanto	MAN3610	Orange	a	f	A	np	np	R	e	d	A	c	g	np	b	A	630	1.2	2.0	2.0	10	3	3	20	400	10	20	5.0	7.6
Monsanto	MAN3620	Orange	a	f	A	np	np	L	e	d	A	c	g	np	b	A	630	1.2	2.0	2.0	10	3	3	20	400	10	20	5.0	7.6
Norbain	NOR1	Red	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	690	1.0	2.1	2.1	15	5.5	5.5	40	750	10	19	3.1	8.4
Norbain	NDP1	Red	a	f	nc	nc	nc	nc	e	d	nc	c	g	nc	b	A	690	1.0	2.1	—	15	5.5	—	40	750	10	19	3.1	8.4
Norbain	NOR1R	Red	a	nc	f	g	nc	e	A	d	c	nc	nc	nc	R	b	690	1.0	2.1	2.1	15	5.5	5.5	40	750	10	19	3.1	8.4
Norbain	NOR1C	Red	a	f	j	nc	nc	L	e	d	nc	c	g	nc	b	A	690	1.0	2.1	2.1	15	5.5	5.5	40	750	10	19	3.1	8.4
Norbain	NOR7	Red	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	690	0.3	2.2	2.2	20	3	3	40	750	10	19	3.1	8.4
Norbain	NOR8	Red	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	690	0.6	2.2	2.2	20	3	3	40	750	10	19	3.1	8.4
Opcoa	SLA1	Red	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	690	1.0	2.1	2.1	15	5.5	5.5	40	750	10	19	3.2	8.4
Opcoa	SLA7	Red	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	690	0.3	2.1	2.1	20	3	3	40	750	10	19	3.2	8.4
Opcoa	SLA11	Green	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	560	0.7	2.6	2.6	40	5.5	5.5	50	1480	10	19	3.2	8.4
Opcoa	SLA21	Yellow	a	f	nc	nc	nc	L	e	d	nc	c	g	nc	b	A	580	0.7	2.6	2.6	40	5.5	5.5	50	1480	10	19	3.2	8.4
Texas	TIL302	Red	a	f	A	np	np	L	e	d	A	c	g	np	b	A	650	0.28	3.4	1.6	20	6	3	30	800	10	19	3.0	6.5
Texas	TIL303	Red	a	A	f	g	np	e	A	d	c	R	np	np	A	b	650	0.28	3.4	1.6	20	6	3	30	800	10	19	3.0	6.5
Xeiton	XAN72	Red	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	697	0.25	1.9	1.9	10	5	5	25	400	10	19	4.6	7.7
Xeiton	XAN52	Green	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	560	0.25	1.9	1.9	10	5	5	25	400	10	19	4.6	7.7
Xeiton	XAN82	Yellow	a	f	A	np	np	L	e	d	nc	c	g	np	b	A	580	0.25	1.9	1.9	10	5	5	25	400	10	19	4.6	7.7

Pin connections and performance data for common-anode 7-segment LED displays.

Explanation of Symbols.

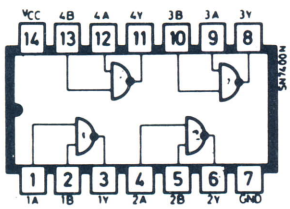
- a-g Segment cathodes.
- L Left-hand decimal point cathode.
- R Right-hand decimal point cathode.
- j Upper decimal point (colon) cathode.
- A Anode.
- nc No connection.
- np No pin.
- λ_p Peak emission wavelength (nanometres).
- I_v Luminous intensity (millicandelas) at specified forward current.
- V_{fs} Segment forward voltage at specified current (volts).
- V_{fd} Decimal point forward voltage drop at specified current (volts).
- @I_f Specified forward current (milliamps).
- V_{rs} Max. segment reverse voltage (volts).
- V_{rd} Max. decimal point reverse voltage (volts).
- I_{av} Max. continuous forward current per segment (milliamps).
- P_{tot} Max. total device dissipation (milliwatts).
- W Width (millimetres).
- H Height (millimetres).
- D Depth (millimetres).
- h Character height (millimetres).

All the parameters listed are measured at 25°C. Values are typical, except for maximum ratings which must not be exceeded.



Note: A prefix to the type number denotes the manufacturer, e.g. **CD** 4001 (RCA), **MC** 14001 (Motorola), **N** 4001 (Signetics), **SCL** 4001 (Solid State Scientific), **SIL** 4001 (Siltek).

7400+ (7403*)



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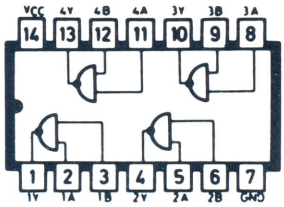
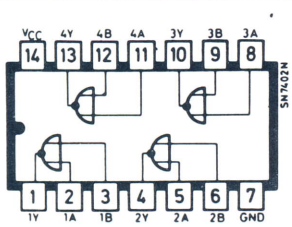
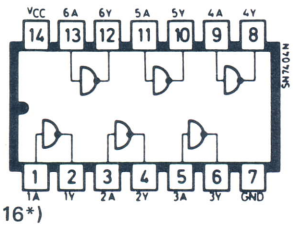


7402+ (7428)



7404+ (7405*, 7406*, 7416*)



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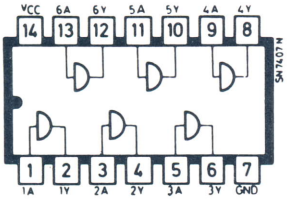

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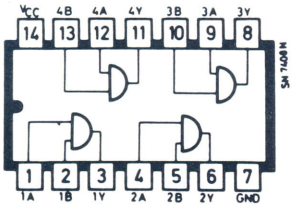
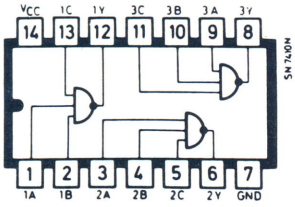
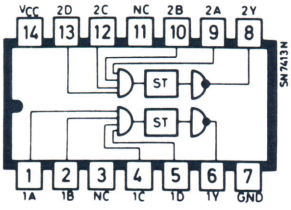


7410+ (7412*)



7413 (7420+, 7440)



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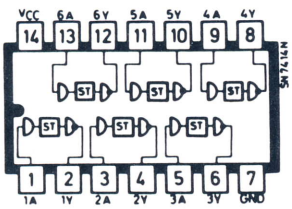

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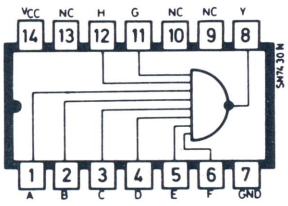

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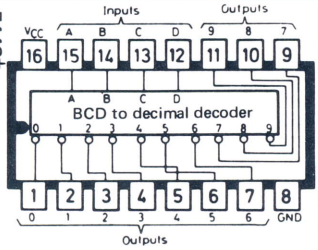

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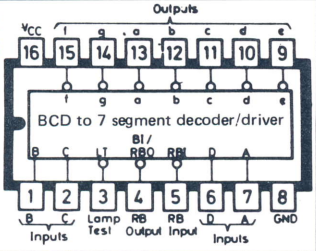

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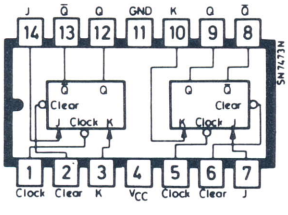

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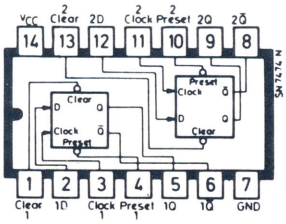

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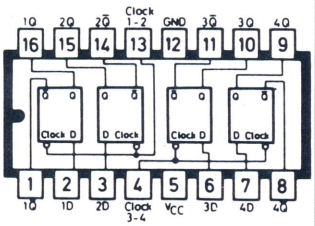

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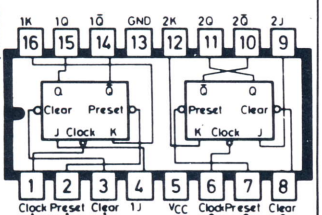

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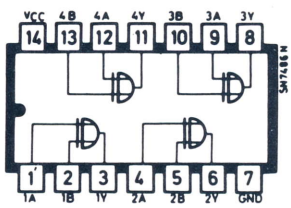

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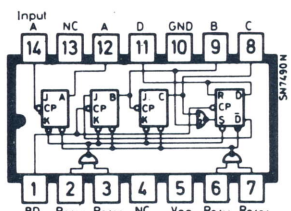

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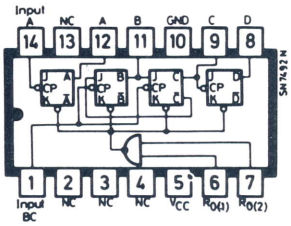

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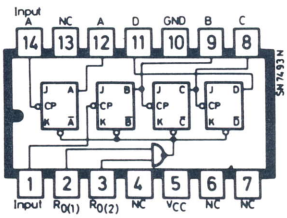

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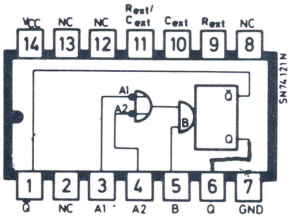

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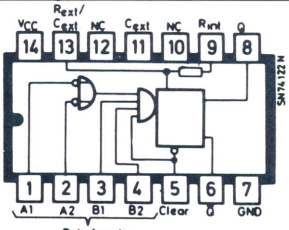

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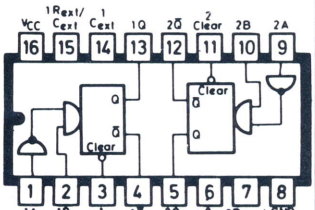

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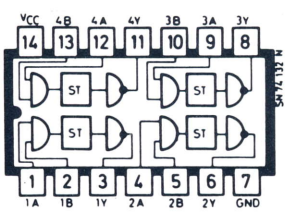

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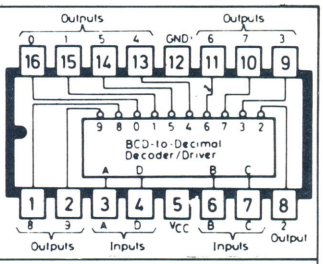

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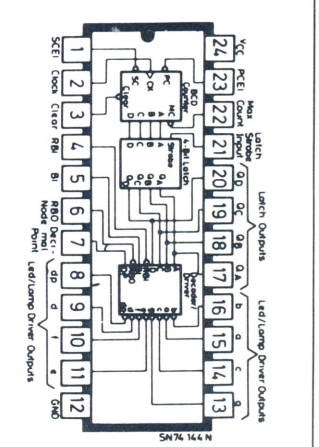

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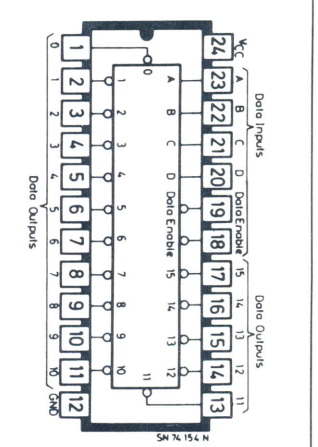

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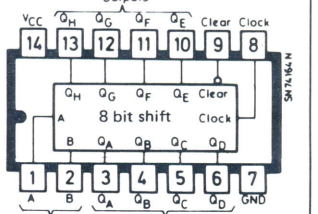

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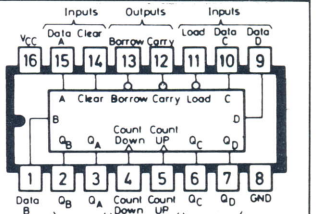

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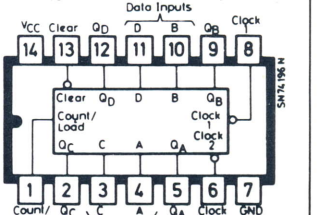
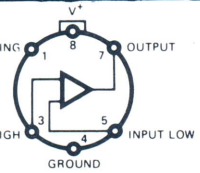


* open collector

+ Pin-compatible CMOS equivalents available from Teledyne Semiconductor and National Semiconductor

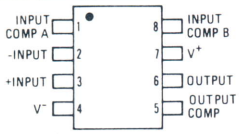
OPAMPS, COMPARATORS

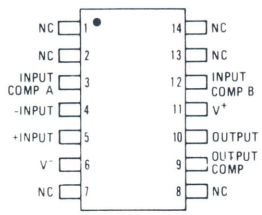
703



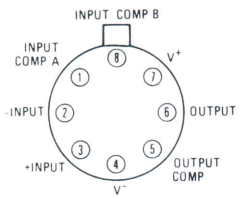
NOTE: Pin 4 connected to case.

709

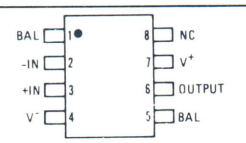


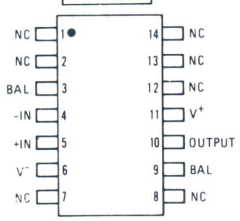


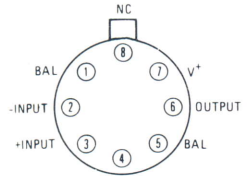
NOTE: Pin 7 connected to bottom of package.



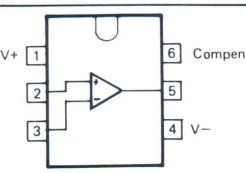
NOTE: Pin 4 connected to case.

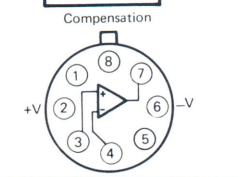


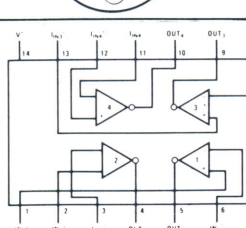




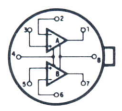
TAA 861 (A)



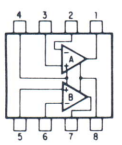




1458 (5558)

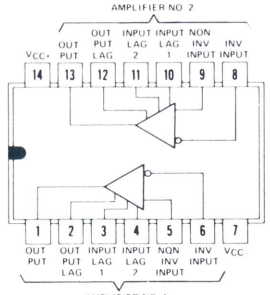


1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V⁻
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V⁺

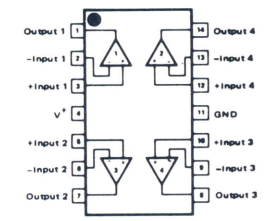


1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V⁻
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V⁺

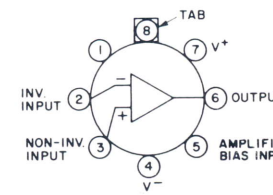
SN 76131 = TBA 231 = μA 739



324

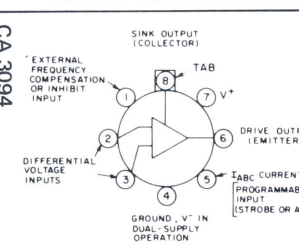


CA 3080



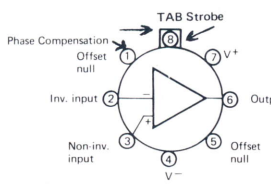
NOTE: Pin 4 is connected to case.

CA 3094



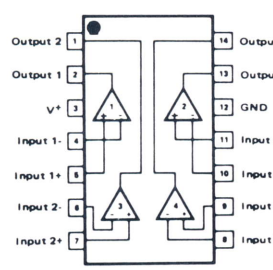
NOTE: Pin 4 is connected to case.

CA 3130



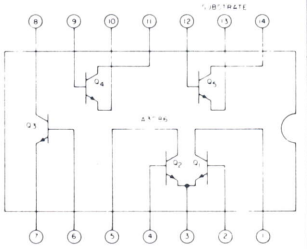
NOTE: Pin 4 is connected to case.

339 (3302)



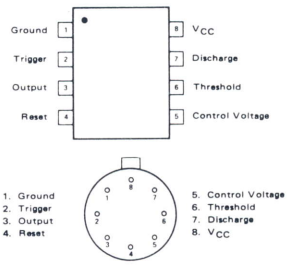
SPECIAL TYPES

CA 3086 = CA 3046

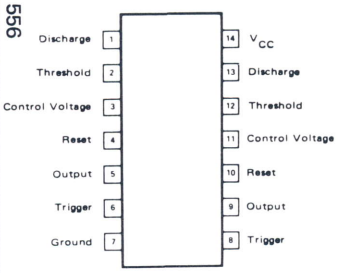


BOTTOM VIEW

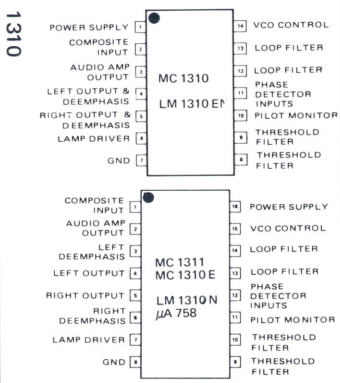
555



556

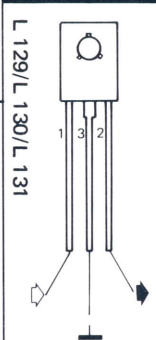


1310

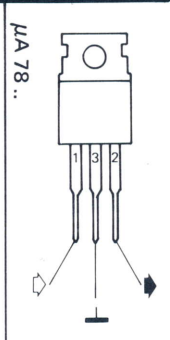


VOLTAGE REGULATORS

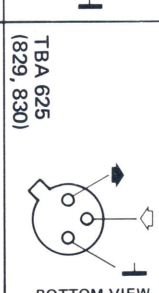
L 129/L 130/L 131



μA 78 ..

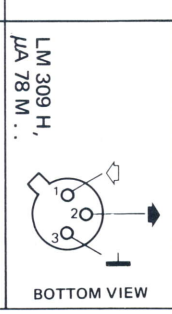


TBA 625 (829, 830)



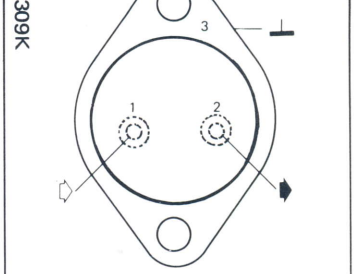
BOTTOM VIEW

LM 309 H, μA 78 M . .

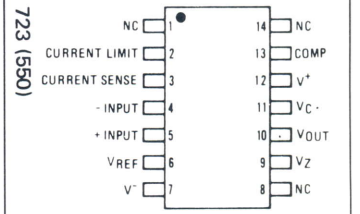


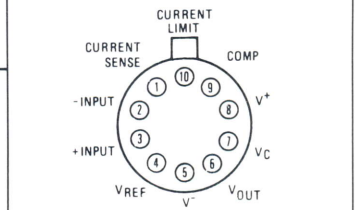
BOTTOM VIEW

LM309K



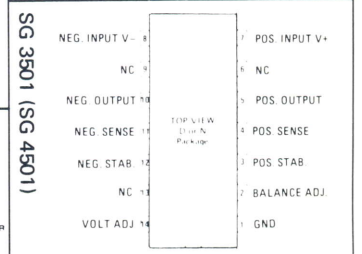
723 (550)

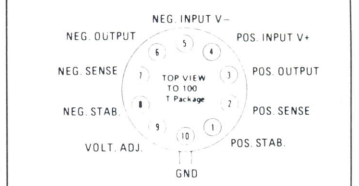




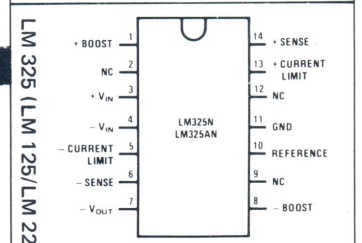
NOTE: On metal can, pin 5 is connected to case.

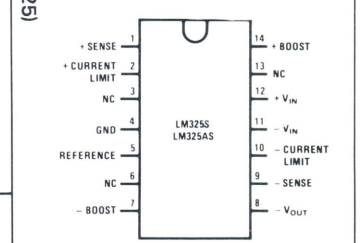
SG 3501 (SG 4501)

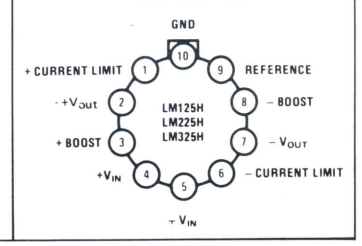




LM 325 (LM 125/LM 225)

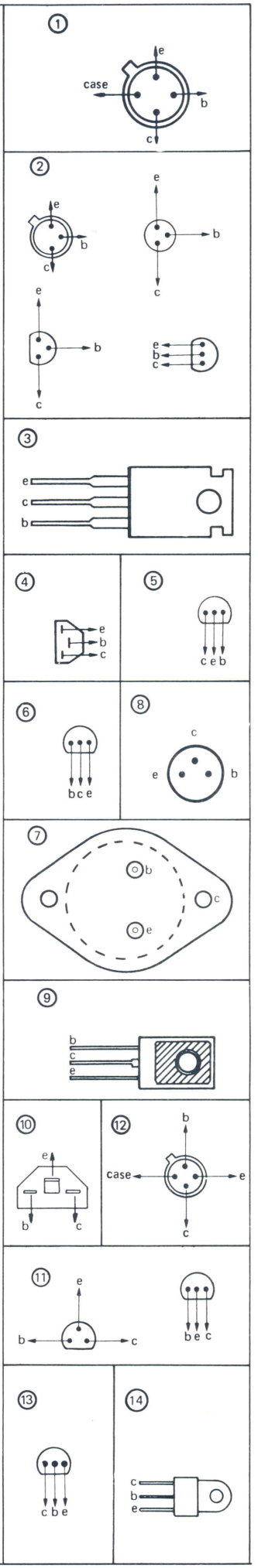






NOTE: All IC's shown top view, unless otherwise stated.

Type	PNP = P NPN = N	V_{CEO} (Volt) 0 = ⩽ 20 00 = 25-40 000 = 45-60 0000 = 65-80 00000 = ⩾ 85	$I_{c(max)}$ (mA) 0 = ⩽ 50 00 = 55-100 000 = 105-400 0000 = 405-2 A 00000 = ⩾ 2 A	P_{max} (mW) not cooled: 0 = ⩽ 300 00 = 305-1000 cooled: 00☆ = 1-10 W 00☆☆ = 10-35 W 00☆☆☆ = ⩾ 40 W	$h_{FE(min)}$ 0 = ⩽ 20 00 = 25-50 000 = 55-120 0000 = ⩾ 125	case nr.	comments	
TUN	N	0	00	0	000			
TUP	P	0	00	0	000			
AC126	P	0	00	00	0000	2		
AF239	P	0	0	0	0	1	grounded base: f	f_T = 700 MHz
BC107	N	000	00	0	000	2		
BC108	N	0	00	0	000	2		
BC109	N	0	00	0	0000	2	low noise	
BC140	N	00	0000	00☆	00	2		
BC141	N	000	0000	00☆	00	2		
BC160	P	00	0000	00☆	00	2		
BC161	P	000	0000	00☆	00	2		
BC182	N	000	000	0	0000	2		
BC212	P	000	000	0	000	2		
BC546	N	0000	00	00	0000	2		
BC556	P	0000	00	00	000	2		
BD106	N	00	00000	00☆☆	00	7		
BD130	N	000	00000	00☆☆	0	7		
BD132	P	000	00000	00☆☆	00	9		
BD137	N	000	0000	00☆	00	9		
BD138	P	000	0000	00☆	00	9		
BD139	N	0000	0000	00☆	00	9		
BD140	P	0000	0000	00☆	00	9		
BDY20	N	000	00000	00☆☆	0	7		
BF180	N	0	0	0	0	1	grounded base:	f_T = 675 MHz
BF185	N	0	0	0	00	12	grounded base:	f_T = 220 MHz
BF194	N	0	0	0	000	10	grounded emitter:	f_T = 260 MHz
BF195	N	0	0	0	000	10	grounded emitter:	f_T = 200 MHz
BF199	N	00	0	00	000	11	grounded emitter:	f_T = 550 MHz
BF200	N	0	0	0	00	1	grounded base:	f_T = 240 MHz
BF254	N	00	0	0	000	11	grounded emitter:	f_T = 260 MHz
BF257	P	00000	00	00	00	2	grounded emitter:	f_T = 90 MHz
BF494	N	0	0	0	000	6	grounded emitter:	f_T = 260 MHz
BFX34	N	000	00000	00	00	2		f_T = 70 MHz
BFX89	N	0	0	0	00	1	grounded emitter:	f_T = 1000 MHz
BFY90	N	0	0	0	00	1	grounded emitter:	f_T = 1000 MHz
BSX19	N	0	0000	0	000	2		
BSX20	N	0	0000	0	000	2		
BSX61	N	000	0000	00	000	2		
HEP51	P	00	0000	00	000	1		f_T = 150 MHz
HEP53	N	00	0000	00	000	1		f_T = 200 MHz
HEP56	N	0	00	00	000	5		f_T = 750 MHz
MJE171	P	000	00000	00☆☆	00	9		
MJE180	N	00	00000	00☆☆	00	9		
MJE181	N	000	00000	00☆☆	00	9		
MJE340	N	00000	0000	00☆☆	00	9		
MPS A05	N	000	0000	00	00	13		
MPS A06	N	0000	0000	00	00	13		
MPS A09	N	0000	0	00	000	13		
MPS A10	N	00	00	00	00	13		
MPS A13	N	00	000	00	0000	13		
MPS A16	N	00	00	00	0000	13		
MPS A17	N	00	00	00	0000	13		
MPS A18	N	000	000	00	0000	13		
MPS A55	P	000	0000	0	00	13		
MPS A56	P	0000	0000	0	00	13		
MPS U01	N	00	00000	00☆	00	14		
MPS U05	N	000	00000	00☆	00	14		
MPS U56	P	0000	00000	00☆	00	14		
MPS2926	N	0	00	00	00	13		f_T = 300 MHz
MPS3394	N	00	00	00	000	13		
MPS3702	P	00	000	00	000	13		f_T = 100 MHz
MPS3706	N	0	0000	00	00	13		
MPS6514	N	00	00	0	0000	13		f_T = 480 MHz
TIP29	N	00	0000	00☆☆	0	3		
TIP30	P	00	0000	00☆☆	0	3		
TIP31	N	00	00000	00☆☆☆	0	3		
TIP32	P	00	00000	00☆☆☆	0	3		
TIP140	N	000	00000	00☆☆☆	0000	7	Darlington	
TIP142	N	00000	00000	00☆☆☆	0000	7	Darlington	
TIP2955	P	000	00000	00☆☆☆	0	3		
TIP3055	N	000	00000	00☆☆☆	0	3		
TIP5530	P	000	00000	00☆☆☆	0	3		
2N696	N	000	0000	00	0	2		
2N706	N	0	0	0	0	2		
2N914	N	0	0000	00	00	2		
2N1613	N	000	0000	00	00	2		
2N1711	N	000	0000	00	000	2		
2N1983	N	00	0000	00	000	2		
2N1984	N	00	0000	00		2		
2N2219	N	00	0000	00	00	2		
2N2222	N	00	0000	00	00	2		
2N2925	N	00	00	0	0000	13		
2N2955	P	00	00	0	0	2	≠ MJE2955, TIP2955!	
2N3054	N	000	00000	00☆☆	00	7		
2N3055	N	000	00000	00☆☆	0	7		
2N3553	N	00	0000	00☆	0	2		f_T = 500 MHz
2N3568	N	000	0000	0	000	13		
2N3638	P	00	0000	0	000	13		
2N3702	P	00	000	00	000	13		
2N3866	N	00	000	00☆	0	2		f_T = 700 MHz
2N3904	N	00	000	0	00	13		
2N3905	P	00	000	00	000	13		
2N3906	P	00	000	00	000	13		
2N3907	N	000	0	0	000	13		
2N4123	N	00	000	0	00	13		
2N4124	N	00	000	0	000	13		
2N4126	P	00	000	0	000	13		
2N4401	N	00	0000	00	0	13		
2N4410	N	0000	000	00	000	13		
2N4427	N	0	000	00☆	0	2		f_T = 700 MHz
2N5183	N	0	0000	00	000	2		



TUP TUN DUG DUS

Wherever possible in Elektor circuits, transistors and diodes are simply marked 'TUP' (Transistor, Universal PNP), 'TUN' (Transistor, Universal NPN), 'DUG' (Diode, Universal Germanium) or 'DUS' (Diode, Universal Silicon). This indicates that a large group of similar devices can be used, provided they meet the minimum specifications listed in tables 1a and 1b.
For further information, see the article 'TUP-TUN-DUG-DUS'.

	type	U_{ceo} max	I_c max	h_{fe} min.	P_{tot} max	f_T min.
TUN	NPN	20 V	100 mA	100	100 mW	100 MHz
TUP	PNP	20 V	100 mA	100	100 mW	100 MHz

Table 1a. Minimum specifications for TUP and TUN.

Table 1b. Minimum specifications for DUS and DUG.

	type	U_R max	I_F max	I_R max	P_{tot} max	C_D max
DUS	Si	25 V	100 mA	1 µA	250 mW	5 pF
DUG	Ge	20 V	35 mA	100 µA	250 mW	10 pF

Table 2. Various transistor types that meet the TUN specifications.

TUN		
BC 107	BC 208	BC 384
BC 108	BC 209	BC 407
BC 109	BC 237	BC 408
BC 147	BC 238	BC 409
BC 148	BC 239	BC 413
BC 149	BC 317	BC 414
BC 171	BC 318	BC 547
BC 172	BC 319	BC 548
BC 173	BC 347	BC 549
BC 182	BC 348	BC 582
BC 183	BC 349	BC 583
BC 184	BC 382	BC 584
BC 207	BC 383	

Table 3. Various transistor types that meet the TUP specifications.

TUP		
BC 157	BC 253	BC 352
BC 158	BC 261	BC 415
BC 177	BC 262	BC 416
BC 178	BC 263	BC 417
BC 204	BC 307	BC 418
BC 205	BC 308	BC 419
BC 206	BC 309	BC 512
BC 212	BC 320	BC 513
BC 213	BC 321	BC 514
BC 214	BC 322	BC 557
BC 251	BC 350	BC 558
BC 252	BC 351	BC 559

Table 4. Various diodes that meet the DUS or DUG specifications.

DUS		DUG
BA 127	BA 318	OA 85
BA 217	BAX13	OA 91
BA 218	BAY61	OA 95
BA 221	1N914	AA 116
BA 222	1N4148	
BA 317		

Table 5. Minimum specifications for the BC107, -108, -109 and BC177, -178, -179 families (according to the Pro-Electron standard). Note that the BC179 does not necessarily meet the TUP specification ($I_{c,max}$ = 50 mA).

	NPN	PNP
	BC 107 BC 108 BC 109	BC 177 BC 178 BC 179
V_{ce_0} max	45 V 20 V 20 V	45 V 25 V 20 V
V_{eb_0} max	6 V 5 V 5 V	5 V 5 V 5 V
I_c max	100 mA 100 mA 100 mA	100 mA 100 mA 50 mA
$P_{tot.}$ max	300 mW 300 mW 300 mW	300 mW 300 mW 300 mW
f_T min.	150 MHz 150 MHz 150 MHz	130 MHz 130 MHz 130 MHz
F max	10 dB 10 dB 4 dB	10 dB 10 dB 4 dB

The letters after the type number denote the current gain:
A: a' (β, h_{fe}) = 125-260
B: a' = 240-500
C: a' = 450-900.

Table 6. Various equivalents for the BC107, -108, . . . families. The data are those given by the Pro-Electron standard; individual manufacturers will sometimes give better specifications for their own products.

NPN	PNP	Case	Remarks
BC 107 BC 108 BC 109	BC 177 BC 178 BC 179		
BC 147 BC 148 BC 149	BC 157 BC 158 BC 159		P_{max} = 250 mW
BC 207 BC 208 BC 209	BC 204 BC 205 BC 206		
BC 237 BC 238 BC 239	BC 307 BC 308 BC 309		
BC 317 BC 318 BC 319	BC 320 BC 321 BC 322		I_{cmax} = 150 mA
BC 347 BC 348 BC 349	BC 350 BC 351 BC 352		
BC 407 BC 408 BC 409	BC 417 BC 418 BC 419		P_{max} = 250 mW
BC 547 BC 548 BC 549	BC 557 BC 558 BC 559		P_{max} = 500 mW
BC 167 BC 168 BC 169	BC 257 BC 258 BC 259		169/259 I_{cmax} = 50 mA
BC 171 BC 172 BC 173	BC 251 BC 252 BC 253		251 . . . 253 low noise
BC 182 BC 183 BC 184	BC 212 BC 213 BC 214		I_{cmax} = 200 mA
BC 582 BC 583 BC 584	BC 512 BC 513 BC 514		I_{cmax} = 200 mA
BC 414 BC 414 BC 414	BC 416 BC 416 BC 416		low noise
BC 413 BC 413	BC 415 BC 415		low noise
BC 382 BC 383 BC 384			
BC 437 BC 438 BC 439			P_{max} = 220 mW
BC 467 BC 468 BC 469			P_{max} = 220 mW
	BC 261 BC 262 BC 263		low noise